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Modeling minority carrier transport and $\mu\tau$ determination in cadmium selenide thin film solar cells

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Modeling minority carrier transport and $\mu\tau$ determination in cadmium selenide thin film solar cells

by

Benjamin H. Reichert

A thesis submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Major: Electrical Engineering (Microelectronics and Photonics)

Program of Study Committee:
Vikram Dalal, Major Professor
Rana Biswas
Jaeyoun Kim

The student author, whose presentation of the scholarship herein was approved by the program of study committee, is solely responsible for the content of this thesis. The Graduate College will ensure this thesis is globally accessible and will not permit alterations after a degree is conferred.

Iowa State University

Ames, Iowa

2019

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ABSTRACT

A simple model for the transport of minority holes in Cadmium Selenide (CdSe) solar cells is presented. Further, via a fitting scheme, the model is shown to permit the subsequent determination of the minority carrier mobility-lifetime ($\mu\tau$) product in CdSe solar cells.

The mobility-lifetime ($\mu\tau$) product is an essential characterization parameter in solar cells, and semiconductors in general. For materials such as CdSe, whose diffusion lengths are insufficient to efficiently collect photogenerated carriers, devices must rely on the presence of an internal electric field to aid in collection – in these devices, transport is noted to be “range dominated”.

As the $\mu\tau$ -product is effectively a metric by which scientists describe the response of the material to a given electric field, its determination, particularly within range-dominated solar cells, is paramount to the greater characterization of the device.

Via our fitting scheme, we characterize the minority-hole $\mu\tau$ of various CdSe devices, and demonstrate its dependence upon device structure and the trap density of states in the material. The transport model is shown to be applicable to both PIN and NIP CdSe device structures. The model goodness-of-fit, in terms of standard deviation, is shown to be in agreement with experimental values, with model values deviating less than 5% from experimental values for the majority of devices measured.

CHAPTER 1. INTRODUCTION

The current academic and industry interest in Cadmium Selenide solar cells stems from several sources. While mainly driven by academic pursuits, the several high-quality solar cell companies have expressed interest in the material, and some of its ‘periodic’ relatives.

Industry Perspective

While CdSe is relatively unexplored in industrial solar applications, Cadmium Telluride (CdTe), a close cousin to CdSe, shows great promise. Several have demonstrated success implementing large scale Cadmium Telluride (CdTe) solar arrays – most notably First Solar’s 290-megawatt deployment in Arizona, and the 550-megawatt Topaz Solar Farm [1]. In many ways, CdTe and CdSe cells are attractive for the same reasons.

Both materials have fairly large bandgaps ($\sim 1.5\text{eV}$ and $\sim 1.74\text{eV}$, respectively), making them ideal for tandem solar cell configurations (as shown below in figure 1.1). In the tandem solar cell, two absorption materials of different bandgap are employed. The large bandgap material absorbs high energy photons, and passes the longer wavelengths. These lower energy photons are then absorbed in the narrow bandgap material. This design tends to increase the overall efficiency of the device, as a greater portion of the solar spectrum is absorbed.

Additionally, both CdSe and CdTe are characterized by very high absorption coefficients - making them ideal for thin film solar cells. Thin absorption layers are often preferred to thicker technologies such as crystalline silicon (c-Si), where films must often be hundreds of microns thick. Note that, for c-Si cells, huge diffusion lengths mean

carriers generated deep within the cell can still be collected, despite the distances they must travel. This is not the case for most thin film solar cells, which rely on high absorption coefficients and field-assisted transport to collect photogenerated carriers. As less material is required when cells are thinner, production costs can be reduced significantly. Additionally, less material means less weight – making thin films of CdTe and CdSe ideal for space-applications (where payload mass is of paramount concern). Lastly, thin cells are flexible, making them ideal for environments where the cells must mirror the curvature of the surface they are mounted on.

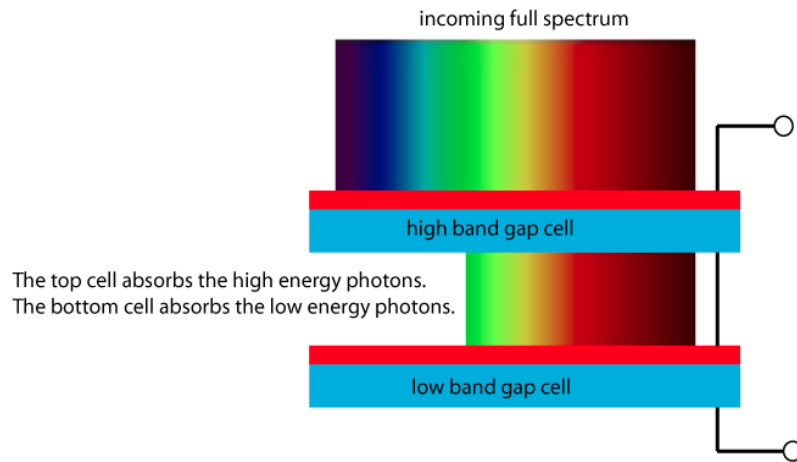


Figure 1.1 Series-Connected Tandem Solar Cell Architecture [2]

Academic Standing

From a purely academic perspective, the fact that CdSe is relatively unexplored makes it an excellent candidate for research. There is a modest repository of publications regarding the material properties of CdSe [3, 4]. In particular, several groups have studied the optical properties of both single crystal, and thin film CdSe. There also exists some literature discussing various methods of CdSe growth and deposition [5].

However, very few research groups have ventured out past discussing these material properties and basic growth techniques. When it comes to employing CdSe thin films as the absorption layer in photovoltaics (PV), there exists minimal academic and industrial discourse.

This is precisely where our research comes into play. Just as previous groups have done, we have, and continue to study the complex material properties of polycrystalline CdSe. In addition to studying these fundamental properties, our group also studies the performance of this material as the absorption layer of PV devices.

Device Structure and Fabrication

While the absorption layer within a device is simply one component in the larger device design, the absorption layer sets the upper-limit to overall device performance. This being the case, all subsequent layers in PV device design are selected based on their ability to assist (or in some cases, simply not hinder) the absorption material.

Unlike crystalline solar cells (e.g. c-Si), CdSe thin films are polycrystalline in nature, and lack long range order. While we have demonstrated crystal order approaching $2\ \mu\text{m}$ for some thin films (via SEM measurements, as shown in figure 1.2 below), the typical grains diameter in our films tends to be approximately $\sim 1, 1.5\ \mu\text{m}$.

The grain size in our CdSe films is highly dependent on the deposition conditions in which the film is grown. Any thermal processes that proceed the deposition of CdSe (post-annealing of the film, CdCl_2 treatment, etc.) influence the film's grain size, as well as other material properties.

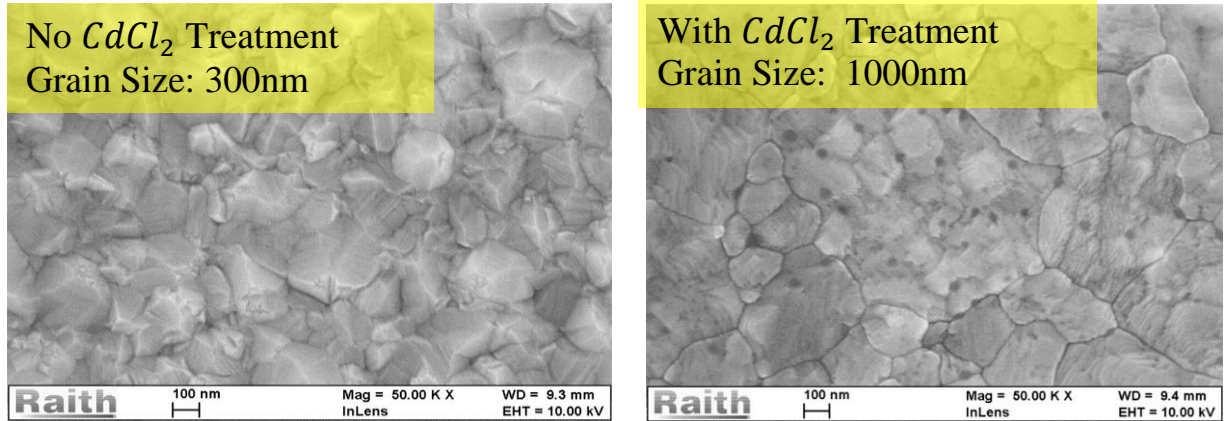


Figure 1.2 SEM imaging of CdSe thin films. Here, we show the impact of process variations on the film grain size.

Due to the absence of long range order in our devices, diffusion lengths tend to be insufficient to collect generated carriers. Therefore, hole and electron transport layers (HTL and ETL, respectively) are employed to increase carrier collection. Due to the depletion field generated at p-n junction of our devices, carrier transport is dominantly characterized by drift transport. Here, the efficiency of our devices is determined by the electric field profile in the absorption layer, and the minority carrier $\mu\tau$ -product. The carrier transport mechanics of our devices is the focus of this thesis, and will be elaborated upon at great length in sections to follow. The importance of the depletion field is mentioned here simply to explain the necessity of the HTL and ETL in our device construction.

Of the several device architectures that have proved promising in our research, this thesis will focus on the two with which we had the most success.

PIN Device Structure

Third level headings (Heading 3 in the Styles ribbon) are bold, not indented, and the first letter of each word capitalized, as with second level headings. If the chapter title or heading is longer than one line, use single spacing between the lines of the title (this is built into the style). Use same font size as other major headings (and bold if other major headings are bold). Be consistent with spacing between chapter title and text for all chapters (this is set in the styles).

Do not leave sub-headings alone at the bottom of a page without any text following it.

You must have at least two lines of text. If necessary, leave extra space at the bottom of the page and place the sub-heading on the next page. This is also set by the heading style by default, and can be adjusted there for ease.

The PIN device structure is detailed in figure 1.3. Additionally, this figure elaborates upon the band structure of this arrangement. The processing of our PIN devices is as follows:

- i.) As is the case with all of our devices, construction starts with a 3rd party glass substrate, on which Fluorine-doped Tin Oxide (FTO) has been deposited. The FTO serves as the electrically conductive cathode contact in the device.
- ii.) Via thermal evaporation, Cadmium Sulfide (CdS), doped n-type with Indium (CdS:In), is grown on top of the FTO cathode. This 30nm CdS:In layer serves as ETL in our device – aiding in the collection of majority electrons from the CdSe absorption layer.

- iii.) Next, $1\mu\text{m}$ of CdSe (intrinsically lightly n-type, $\sim 10^{15}/\text{cm}^3$) is thermally evaporated on top of the ETL. This $1\mu\text{m}$ thin film of polycrystalline CdSe serves as the absorption layer of our device.
- iv.) The CdSe layer is then treated with a liquid Cadmium-Chloride solution (CdCl_2). Experiments conducted in tandem with this thesis have demonstrated that this CdCl_2 treatment acts to decrease the defect density in CdSe, however the details of this mechanism are not the focus of this thesis, and thus will not be elaborated upon.
- v.) Next, the HTL is obtained via spin-coating poly(3,4-ethylenedioxythiophene) (PEDOT) onto the CdSe layer. PEDOT is a highly conductive p-type polymer that acts to induce large depletion field in the lightly n-type CdSe layer.
- vi.) Finally, 70 nm of Indium Tin Oxide (ITO) is sputtered on top of the PEDOT HTL. This highly conductive oxide serves an excellent top contact (anode) to the device. Additionally, ITO virtually transparent to the solar spectrum, thus losses due to absorption in the contact are

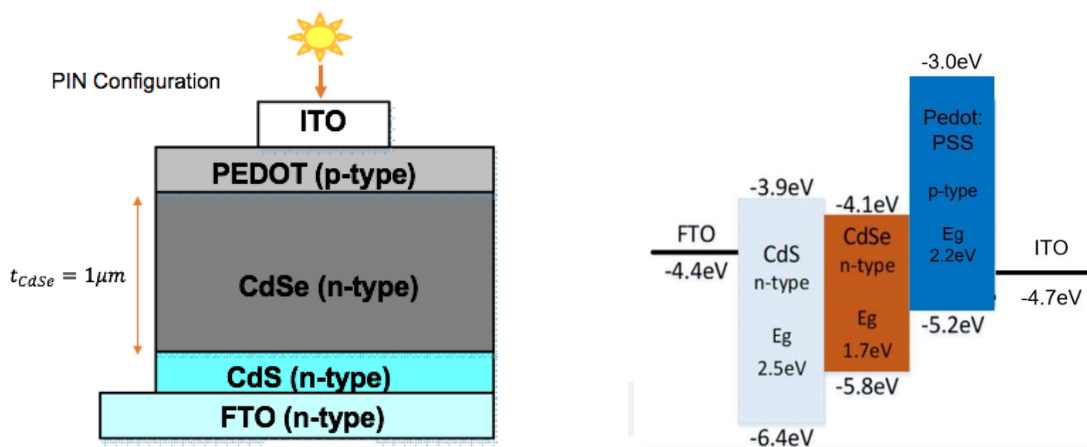


Figure 1.3 PIN device architecture and band structure [6]

As figure 1.3 demonstrates, the device is operated in the “PIN” or “substrate” configuration. This means that light is incident to the “top” surface of the solar cell (i.e. incident light hits the ITO layer first). Here, ITO and PEDOT are virtually transparent to the AM1.5 solar spectrum. Additionally, we note that PEDOT is characterized by a large bandgap. As such, incident light can pass thru the top contact and p-layer of the structure, to be absorbed in the intended region (the CdSe layer).

NIP Device Structure

The NIP device structure is detailed in figure 1.4. Additionally, this figure elaborates upon the band structure of this arrangement as well. The processing of our NIP devices is as follows:

- i.) Again, construction starts with a 3rd party glass substrate, on which Fluorine-doped Tin Oxide (FTO) has been deposited. The FTO serves as the electrically conductive cathode contact in the device.
- ii.) Via thermal evaporation, Cadmium Sulfide, doped n-type with Indium (CdS:In), is grown on top of the FTO cathode. This 30nm CdS:In layer serves as ETL in our device – aiding in the collection of majority electrons from the CdSe absorption layer.
- iii.) Next, 500 nm of CdSe (intrinsically lightly n-type) is thermally evaporated on top of the ETL. This 500 nm thin film of polycrystalline CdSe serves as the absorption layer of our device.
- iv.) The CdSe layer is then treated with a liquid Cadmium-Chloride solution (CdCl₂).
- v.) Next, the HTL is obtained via spin-coating poly(3-hexylthiophene-2,5-diyl) (P3HT) onto the CdSe layer. Similar to PEDOT, P3HT is a highly

conductive polymer that acts to induce large depletion field in the lightly n-type CdSe layer.

- vi.) Finally, gold (Au) is deposited on top of the P3HT HTL. Electrically, gold serves as an excellent top contact.

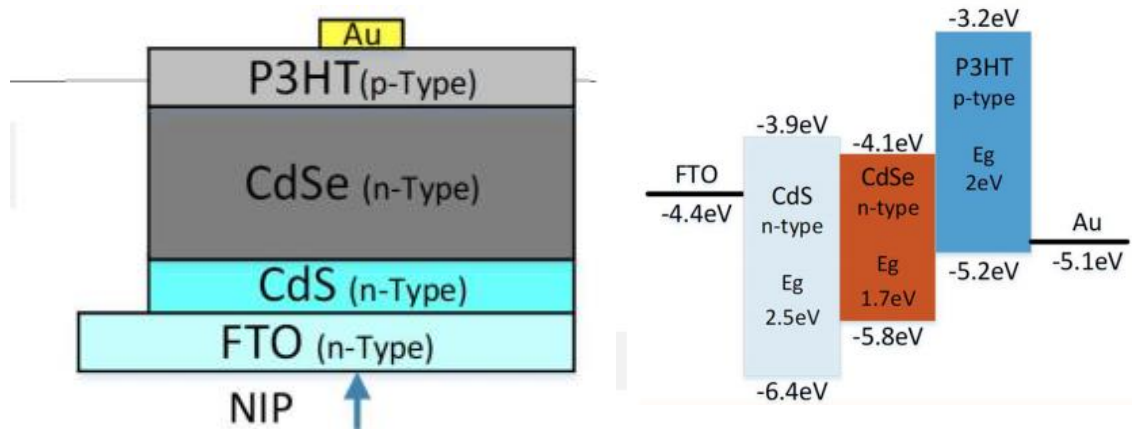


Figure 1.4 NIP device architecture and band structure [6]

There are several key differences between the operation the PIN and NIP device architectures. Most significantly, the NIP device is operated in “superstrate” configuration. This means that incident light is directed up thru the bottom of the cell, as indicated by the arrow in figure 1.4 above. The superstrate configuration is a necessity for this device, as the Au/P3HT complex absorbs quite strongly. The larger bandgap of CdS (2.5eV) ensures that most light incident here will pass thru to be absorbed in the desired layer (CdSe). Therefore, in order to obtain higher device efficiencies in this architecture, light must be directed up thru the “bottom” of the device.

Concluding Comments

As is demonstrated by the descriptions above, these two device structures are distinctly different in both construction and operation. These device architectures were selected to speak to the validity of the transport model presented in this thesis. Here, we seek to demonstrate a robust description of CdSe carrier transport, independent of device configuration and construction.

CHAPTER 2. MODEL THEORY

In the sections to follow, we demonstrate a model by which device internal quantum efficiency (IQE) can be numerically determined for PIN and NIP CdSe devices. With the quantity of variables running around in these sections, it is important to outline precisely what is to be treated as “known”, and what is to be determined via the model.

The optical absorption coefficient of CdSe (α_{CdSe}) is determined via independent spectrophotometry measurements, coupled with literature values [3,4]. Device parameters such as built-in voltage (V_{bi}) and absorption layer donor concentration ($N_{D,CdSe}$) are obtained via Capacitance-Voltage (CV) measurements. Device thickness is controlled to a high degree of accuracy in the deposition process, and therefore is known.

When provided these material/device parameters, the model constructs an analytical IQE vs. $V_{applied\ bias}$ curve for a given wavelength of incident light. Generally, these curves demonstrate increased IQE at simulated reverse biases, and decreased IQE at forward biases. However, the precise nature of these curves depends heavily on the device structure, so generalizations past this observation are of limited use. This will be discussed heavily in the results section of this thesis.

The only “unknown” in our IQE expression is the $\mu_p\tau_p$ of the CdSe layer. Herein lies the true value of our model. We swing the $\mu_p\tau_p$ value employed in the determination of analytical IQE and compare this calculated value to the experimentally measured IQE for the device, at that wavelength and applied bias. Therefore, the CdSe minority carrier mu-tau product can be determined by finding the $\mu_p\tau_p$ value that provides greatest agreement between the analytical and experimental IQE values.

Origin

The origin of our model is rooted in a few simple observations regarding the nature of the charge transport within our devices. As has been mentioned above, our CdSe absorption layer is intrinsically n-type. This observation greatly simplifies the analysis to follow, as author et al have demonstrated that minority carriers govern the generation and recombination processes in their study of ambipolar transport [7].

For devices in which carrier transport and collection is throttled by recombination processes, modeling of only minority carrier transport is sufficient for describing the overall device performance. Thus polycrystalline CdSe devices, in which transport is limited by defect states (primarily from grain boundaries and defect states in the film), we must study the nature of minority-hole transport.

We begin our analysis with the standard definition of “hole current density”, as provided below:

$$J_p = q\mu_p \epsilon p - qD_p \frac{dp}{dx} \quad (2.1)$$

In expressions to follow, μ_p [$\frac{cm^2}{V \cdot s}$] is the hole mobility, ϵ [$\frac{V}{cm}$] is the electric field, p [$\frac{1}{cm^3}$] is the volumetric hole concentration, and D_p [$\frac{cm^2}{s}$] is the diffusion coefficient of holes in CdSe. It is clear that in equation 2.1, current density is a function of both drift transport and diffusion transport.

From equation 2.1, combined with the generation (G) and recombination (R) terms, we construct the minority hole continuity equation, as given below:

$$\frac{dp}{dt} = -\frac{1}{q} \cdot \frac{dJ_p}{dx} + G - R \quad (2.2)$$

Several simplifications can be presumed when analyzing equation 2.2. Chiefly, in the small signal approximation, we must maintain charge neutrality, therefore $\frac{dp}{dt} = \frac{dn}{dt} = 0$. If we consider a small-signal quantity of Δp holes generated within the bulk of the n-type semiconductor, the subsequent expression for minority holes becomes:

$$\frac{d\Delta p}{dt} = -\frac{1}{q} \cdot \frac{dJ_p}{dx} - \frac{\Delta p}{\tau_p} = 0 \quad (2.3)$$

For regions where diffusion dominates hole transport, current density simply becomes: $J_p = J_{p,diff} = -qD_p \frac{dp}{dx}$. Applying this simplified current density to equation 2.3 above yields:

$$D_p \frac{d^2\Delta p}{dx^2} - \frac{\Delta p}{\tau_p} = 0 \quad (2.4)$$

Finally, solving the second order differential equation above (equation 2.4) and applying necessary boundary conditions yields an expression for the decay of generated holes, as they diffuse from the region of generation and recombine:

$$\Delta p(x) = \Delta p(0) \cdot e^{-x/L_p} \quad (2.5)$$

Above, the diffusion length (L_p) is defined as: $L_p = \sqrt{D_p \tau_p}$ [cm]. Additionally, by the Einstein relation, diffusion length can also be defined as a function of the $\mu\tau$ -product, where $L_p = \sqrt{\frac{kT}{q} \cdot \mu_p \tau_p}$. We find that this formulation for diffusion length will come in handy in sections to follow.

We can derive a similar expression for the decay of generated holes where transport is dominated by an electric field (i.e. drift transport). In this case, current density simplifies to $J_p = J_{p,drift} = q\mu_p \epsilon p$. Applying this simplified expression to equation 2.3 yields:

$$\mu_p \varepsilon \frac{d\Delta p}{dx} - \frac{\Delta p}{\tau_p} = 0 \quad (2.6)$$

Again, solving the differential equation and applying necessary boundary conditions to equation 2.6 above, we obtain an expression for the decay of generated holes (Δp), as they drift from the region of generated and recombine:

$$\Delta p(x) = \Delta p(0) \cdot e^{-x/R_p} \quad (2.7)$$

Where Range (R_p) is defined as: $R_p = \mu_p \tau_p \varepsilon$ [cm].

Here, note that under careful analysis, we observe the expression for drift transport above makes one fundamental assumption. The electric field term ε has been pulled out of the derivative of drift current density ($J_{p,\text{drift}}$) in equation 2.6, therefore equations 2.6 and 2.7 above assume a constant electric field profile within the absorbing layer. In other words, equations 2.6 and 2.7 necessitate that $\frac{d\varepsilon}{dx} = 0$ within the absorbing semiconductor.

Lastly, one final expression is required to begin constructing our model. The mechanism by which the pulse of holes Δp is generated is, of course, incident photon flux ' Γ ', with the units of [$\frac{\text{photons}}{\text{cm}^2}$]. Accounting for absorption as a function of penetration depth ' x ' into the semiconductor, $\Gamma(x, \lambda)$ is defined as follows:

$$\Gamma(x, \lambda) = \Gamma_0(\lambda) \cdot e^{-\alpha(\lambda) \cdot x} \quad (2.8)$$

Above, $\Gamma_0(\lambda)$ signifies the photon flux present at $x = 0$, where absorption has yet to decrease the flux. The 'absorption coefficient' α [$\frac{1}{\text{cm}}$], is a material constant, and is taken to be known in this analysis. By simply rearranging equation 2.8, we obtain the ratio of remaining photons to the original quantity present, a useful expression in the section to follow. The ratio is provided explicitly below:

$$\frac{\Gamma(x,\lambda)}{\Gamma_0} = e^{-\alpha(\lambda) \cdot x} \quad (2.9)$$

Transport Model: The Ideal PIN Case

The ideal intrinsic (i-layer) is taken to be undoped, and devoid of trap states.

Therefore, with no dopant atoms to ionize, the intrinsic layer is presumed to be devoid of mobile charge carriers. Employing Poisson's theorem:

$$\frac{d\varepsilon(x)}{dx} = \frac{\rho(x)}{\epsilon_0} \quad (2.10)$$

We find that within the i-layer, the electric field profile $\varepsilon(x)$ is constant, as the charge density within the i-layer is zero ($\rho_{i-layer} = 0$). Based on this simple observation, we can visualize the charge density ($\rho(x)$ vs. x), the electric field profile ($\varepsilon(x)$ vs. x), and the band-structure of the ideal PIN solar cell, as demonstrated below in figure 2.1:

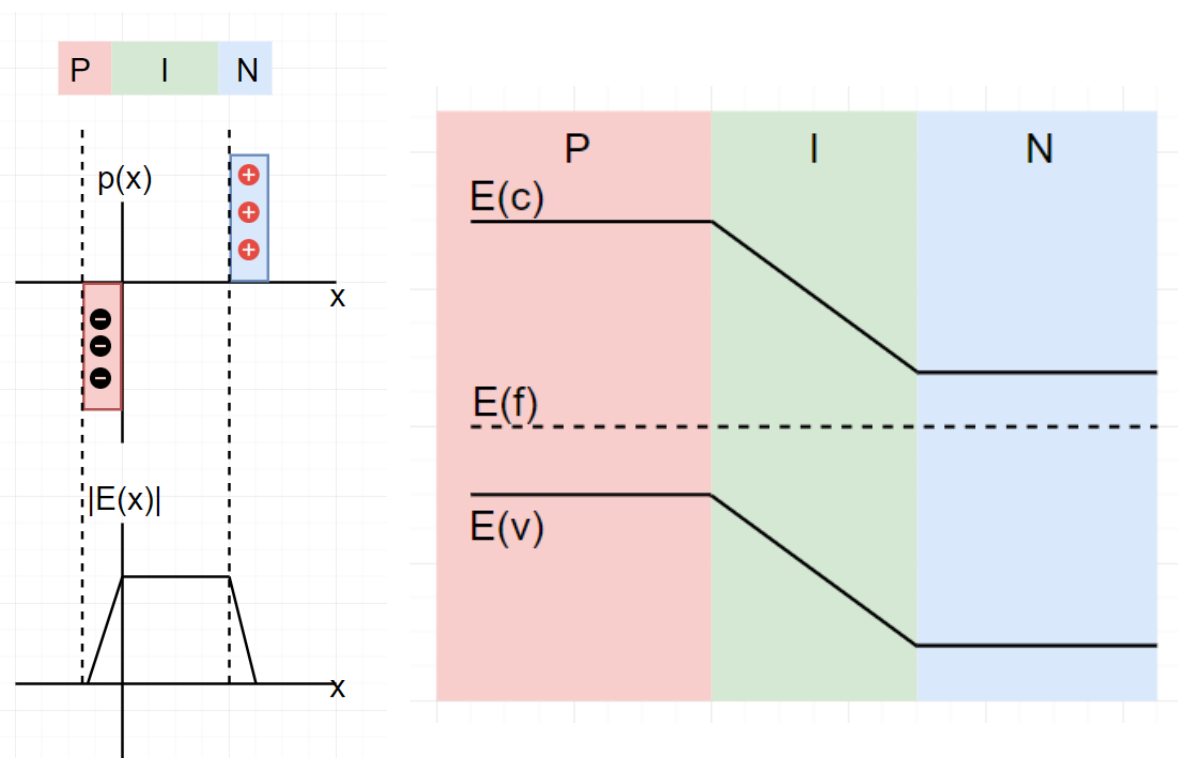


Figure 2.1 The ideal PIN device charge distribution, electric field profile, and band structure

As illustrated in figure 2.1 above, any carrier generated within the i-layer is subject to a uniform electric field. The electric field's spatial independence greatly simplifies our final expression for minority hole capture. It is common to define carrier capture in terms of 'internal quantum efficiency' or IQE. IQE is defined simply as:

$\frac{\# \text{ photons absorbed}}{\# \text{ of carriers collected}}$. Employing equations 2.7 and 2.9, we express the total IQE of the ideal PIN solar cell as follows:

$$IQE_{Tot} = IQE_{drift}(\lambda) = \alpha(\lambda) \int_0^t e^{-\alpha x} \cdot dx \cdot e^{-\frac{x}{R_p}} \quad @ \quad \varepsilon \geq \varepsilon_{boundary} \quad (2.11)$$

$$IQE_{Tot} = IQE_{diffusion}(\lambda) = \alpha(\lambda) \int_0^t e^{-\alpha x} \cdot dx \cdot e^{-\frac{x}{L_p}} \quad @ \quad \varepsilon \geq \varepsilon_{boundary} \quad (2.12)$$

We note in equations 2.11 and 2.12 above, 't' designates the thickness of the i-layer.

These expressions presume that the p-layer and n-layer are sufficiently thin and have high bandgaps, such that absorption occurs exclusively within the i-layer.

We discriminate between expressions 2.11 and 2.12 above via the boundary field condition ($\varepsilon_{boundary}$), which is defined below:

$$\varepsilon_{boundary} = \frac{kT/q}{L_p} \quad (2.13)$$

This boundary condition is derived via little more inspection. Clearly, if the depletion field is greater than the quotient of the system thermal voltage (kT/q) and the minority carrier diffusion length (L_p), then drift transport will dominate hole collection. Otherwise, for cases where $L_p > R_p$, the material diffusion length will govern minority hole collection.

For the ideal PIN cell, the integrations for equations 2.11 and 2.12 are trivial to solve. Neither L_p nor R_p are functions of x , therefore the following closed-form solutions are attained:

$$IQE_{diffusion}(\lambda) = -\frac{\alpha}{\alpha + \frac{1}{L_p}} \cdot [e^{-t(\alpha + \frac{1}{L_p})} - 1] \quad (2.14)$$

$$IQE_{drift}(\lambda) = -\frac{\alpha}{\alpha + \frac{1}{R_p}} \cdot [e^{-t(\alpha + \frac{1}{R_p})} - 1] \quad (2.15)$$

Above we note that, provided the i-layer is thick enough, the solutions above reduce further to $IQE_{diffusion}(\lambda) = \frac{\alpha}{\alpha + \frac{1}{L_p}}$ and $IQE_{drift}(\lambda) = \frac{\alpha}{\alpha + \frac{1}{R_p}}$. These are the expressions commonly found in undergraduate textbooks.

Transport Model: CdSe PIN Modifications

As stated in previous sections, we know our CdSe thin films to n-type doped, intrinsically. Via C-V measurements (which will be elaborated upon in sections to follow), we obtain CdSe donor doping values on the order of $N_D \sim 10^{15}/cm^3$. Additionally, both PEDOT and P3HT (our p-type HTLs) are highly conductive polymers, with an effective ‘fermi sea’ of holes available from either of these HTLs. Thus, the p/i interface can be approximated as a Schottky-Mott barrier (a metal-semiconductor junction).

Further, with an effectively infinite charge density of holes available in either of these p-layers, we can accurately approximate the depletion field to extend exclusively into the CdSe i-layer. Due to the abundance of charge available in the p-layer, this depletion width does not extend appreciably into the PEDOT or P3HT (i.e. $-x_p \approx 0$).

Applying the observations made above, we can visualize the charge density, electric field profile, and band-structure at the p/i interface as shown in figure 2.2 below:

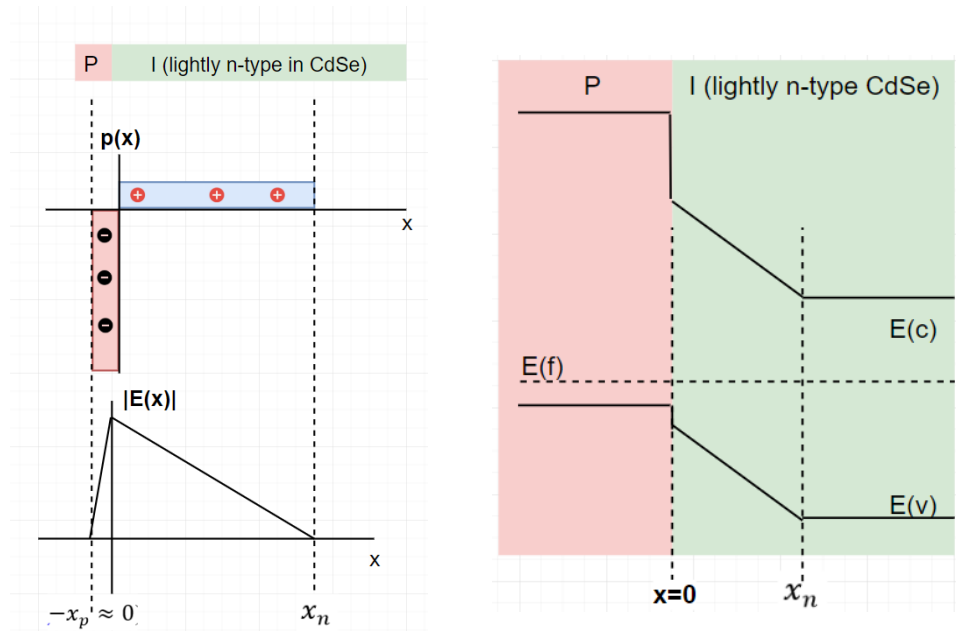


Figure 2.2 CdSe PIN device charge distribution, electric field profile, and band structure

Figure 2.2 above illustrates the triangular profile of $\varepsilon(x)$. The electric field converges to a value of 0 at the end of the depletion width, i.e. $\varepsilon(x) = 0 @ x = x_n, W_d$. Additionally, we find this position by applying the single sided depletion width approximation:

$$W_{d,1-sided} = \sqrt{\frac{2\varepsilon(V_{bi}+V_{Applied})}{q \cdot N_D}} \quad (2.16)$$

Experimentally, both the built-in voltage (V_{bi}) and the CdSe doping density (N_D) are obtained via CV measurement. Applying a reverse bias to the sample serves to increase the depletion width, while forward biases reduce the depletion region.

The simple nature of our electric field approximation allows us to easily define $\varepsilon(x)$ as a function of device parameters. The area under the triangular field must yield the

net voltage, i.e. : $|V_{bi} + V_{Applied}| = \left| \int_0^{W_{d,1-sided}} \varepsilon(x) dx \right|$. Therefore the expression for $\varepsilon(x)$ in our system is derived as follows:

$$\varepsilon(x) = -\frac{2(V_{bi}+V_{Applied})}{W_{d,1-sided}^2} \cdot x + \frac{2 \cdot (V_{bi}+V_{Applied})}{W_{d,1-sided}} \quad (2.17)$$

Lastly, we must distinguish between regions of diffuse transport and drift transport within the device. In regions where the electric field is weak or non-existent, we express minority transport (and therefore IQE) is driven by diffusion. In regions where the field is dominant, IQE is characterized by drift of minority carriers. Just as was done in the previous section, we distinguish between these two regions via the $\varepsilon_{boundary}$ condition (equation 2.13). We define the position at which the system transitions between these two modes of transport as the “effective depletion width”, W'_d :

$$\varepsilon(x = W'_d) = \varepsilon_{boundary} \quad (2.18)$$

Combining expressions 2.15 and 2.16, we obtain an expression for the effective depletion width W'_d :

$$W'_d = -\frac{\varepsilon_{boundary} \cdot W_{d,1-sided}^2}{2(V_{bi}+V_{Applied})} + W_{d,1-sided} \quad (2.19)$$

Figures 2.3, 2.4, and 2.5 below illustrate the PIN system, as we have defined it thus far.

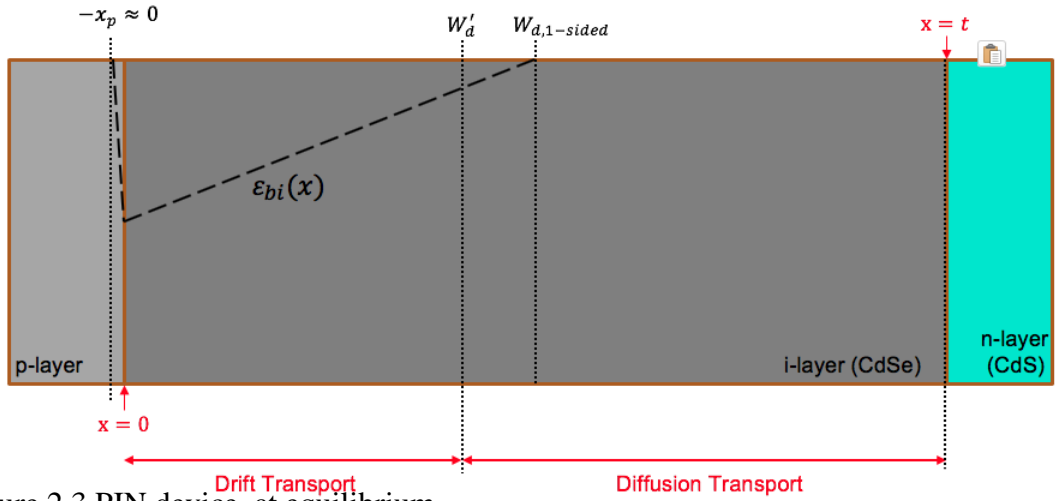


Figure 2.3 PIN device, at equilibrium

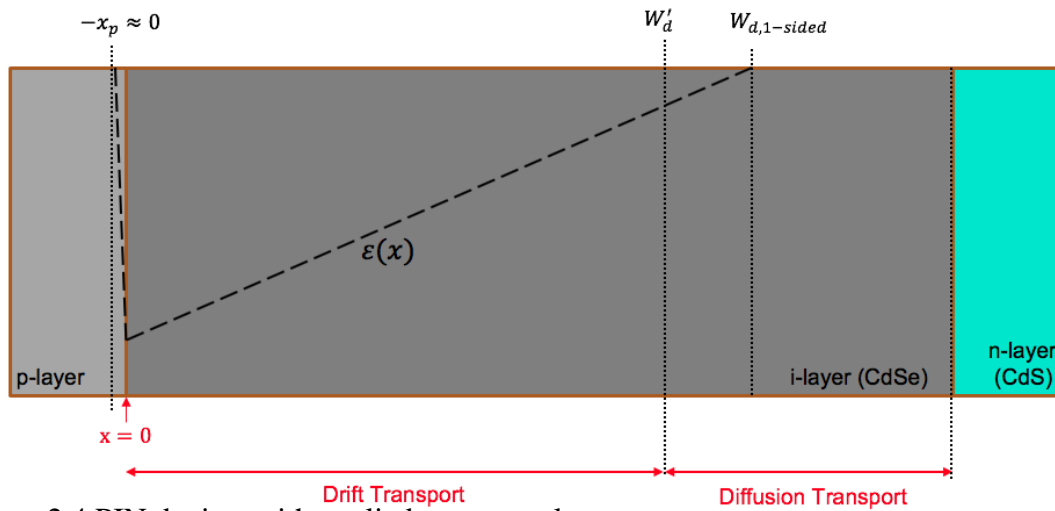


Figure 2.4 PIN device, with applied reverse voltage

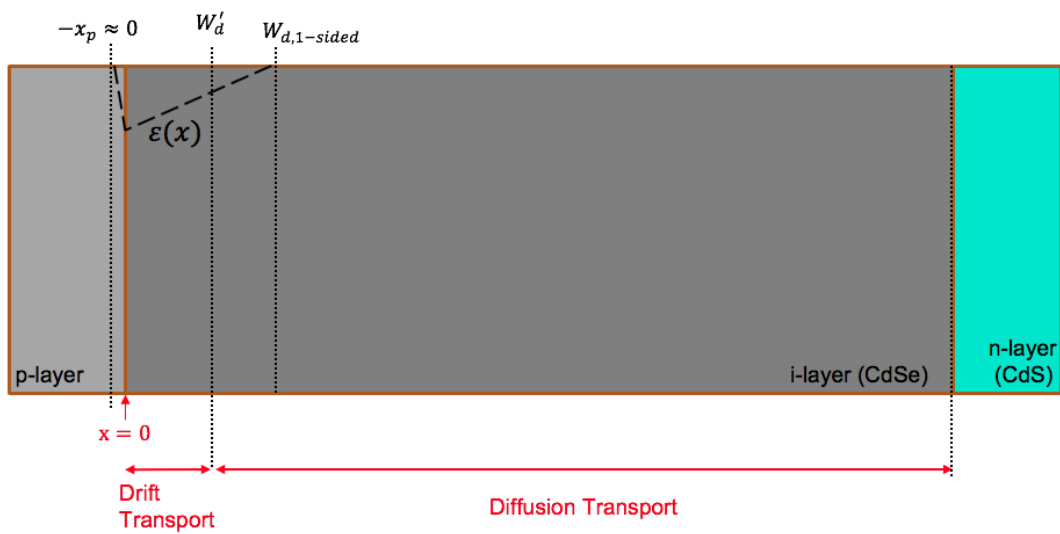


Figure 2.5 PIN device, with applied forward voltage

to the p-layer for collection. The full model for PIN IQE must be expressed numerically then, as shown below:

$$\Delta p_0 = IQE_{diffusion} = \alpha \int_{W'_d}^t e^{-\alpha x} \cdot e^{-\frac{x-W'_d}{L_p}} dx \quad (2.22)$$

$$\Delta p_{n-1} = \left[\Delta p_{n-2} \cdot e^{-\frac{\Delta x}{\mu_p \tau_p \varepsilon(x)}} \right] + \left[\alpha \cdot e^{-\alpha x} \cdot \Delta x \cdot e^{-\frac{\Delta x}{2\mu_p \tau_p \varepsilon(x)}} \right] @ 99 \geq n \geq 2 \quad (2.23)$$

$$IQE_{Total} = \Delta p_{99} \quad (2.24)$$

Here, the spatial distance from $W'_d \rightarrow 0$ is divided into “n” equal partitions, each partition with a finite width of Δx . The width of each partition is given by $\Delta x = \frac{W'_d}{n}$. The value of the electric field is determined by evaluating equation 2.17 at discrete positions, where $x = W'_d - (\Delta x \cdot n)$. Generally, we find that $n = 100$ provides sufficient evaluation points for the numerical integration.

Concluding Comments

Via equations 2.22, 2.23, 2.24, the internal quantum efficiency of a given PIN device is modeled. Practically, this is done within a MATLAB script. Thru this method, we obtain a family of model curves (IQE vs. $V_{Applied}$), which are compared to measured curves. By sweeping thru a set of potential $\mu_p \tau_p$ values, we determine the $\mu_p \tau_p$ yielding the best agreement between the model and experimental data. Therefore, from this method, we are able to determine, within reasonable accuracy, what the minority carrier $\mu_p \tau_p$ product is for our CdSe devices.

The careful reader will also notice that within this model, we have not accounted for the junction effects at the CdSe/CdS interface. In order to maintain relative simplicity of this model, this junction has been ignored. Additionally, the relative proximity of fermi levels in our n-type CdS and intrinsic CdSe ensures that any band-bending and depletion

effects will be mild at this interface. Therefore, we expect the electric field and subsequent carrier drift to be characterized dominantly by the p/i interface.

Transport Model: CdSe NIP Modifications

Much of the derivation for the NIP transport model is identical to that of the PIN structure. The formulations for the depletion width ($W_{d,1-sided}$), the electric field profile $\varepsilon(x)$, and the effective depletion width (W'_d) are identical to the PIN expressions (equations 2.16, 2.17, & 2.19, respectively).

The fact that the photon flux is incident to the back contact of the device simply necessitates some minor adjustments to the bounds of integration in our expressions. The NIP generation process is detailed below in figure 2.7:

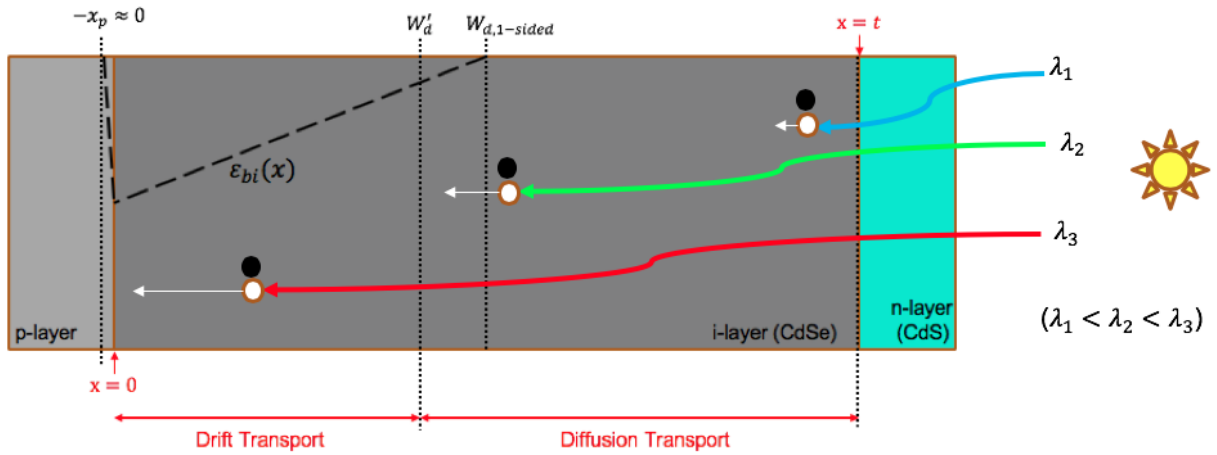


Figure 2.7 NIP device generation process

For the NIP structure, our diffusion expression must be modified as follows:

$$IQE_{diffusion} = \alpha \int_0^{t-W'_d} e^{-\alpha x} \cdot e^{-\frac{(t-W'_d)-x}{L_p}} dx \quad (2.25)$$

While the numerical integration scheme is adjusted as well:

$$\Delta p_0 = IQE_{diffusion} = \alpha \int_0^{t-W'_d} e^{-\alpha x} \cdot e^{-\frac{(t-W'_d)-x}{L_p}} dx \quad (2.26)$$

$$\Delta p_{n-1} = \left[\Delta p_{n-2} \cdot e^{-\frac{\Delta x}{\mu p \tau_p \epsilon(x)}} \right] + \left[\alpha \cdot e^{-\alpha(t-x)} \cdot \Delta x \cdot e^{-\frac{\Delta x}{2\mu p \tau_p \epsilon(x)}} \right] \quad @99 \geq n \geq 2 \quad (2.27)$$

$$IQE_{Total} = \Delta p_{99} \quad (2.28)$$

Just as was the case for the PIN structure, we partition the spatial distance from $W'_d \rightarrow 0$ into equal 'slices' of Δx . Again, we find that $n=100$ partitions proves sufficient evaluation points for the numerical integration.

CHAPTER 3. MEASUREMENTS

The accuracy of our model, and subsequent mu-tau determination depends heavily on the measurement of several device parameters prior to conducting the IQE Vs. $V_{applied\ bias}$ measurement. Namely, Capacitance-Voltage data, EQE Vs. λ data, and device reflectivity measurements are all required to accurately determine the device mu-tau product.

Capacitance – Voltage

The Mott-Schottky measurement is a popular method by which to characterize semiconductor junctions. In particular, we easily derive the device built-in voltage (V_{bi}) and donor doping concentration ($N_{D,CdSe}$). Rearranging the one-sided junction formulation provided in equation 2.16, we can plot $\frac{1}{C^2}$ as function of applied bias voltage, otherwise known as the Mott-Schottky plot. The C Vs. V_{bias} relationship is given below:

$$\frac{1}{C^2} = \frac{2}{\epsilon q A^2 N_D} (V_{bi} + V_{Reverse\ Bias}) \quad (3.1)$$

Where the slope reveals sample doping density, while the x-intercept returns the built-in voltage of the junction.

PIN CV Measurement

The device was kept in the dark for ~30 minutes prior to the measurement to ensure the recombination of any latent photogenerated carriers. The PIN device was swept from -1V (forward bias) to +1V (reverse bias), with 100mV steps in-between each sample. A small-signal AC frequency of 50kHz was employed (to generate the requisite $\frac{dQ}{dV}$). The measurement results are presented below in figure 3.1:

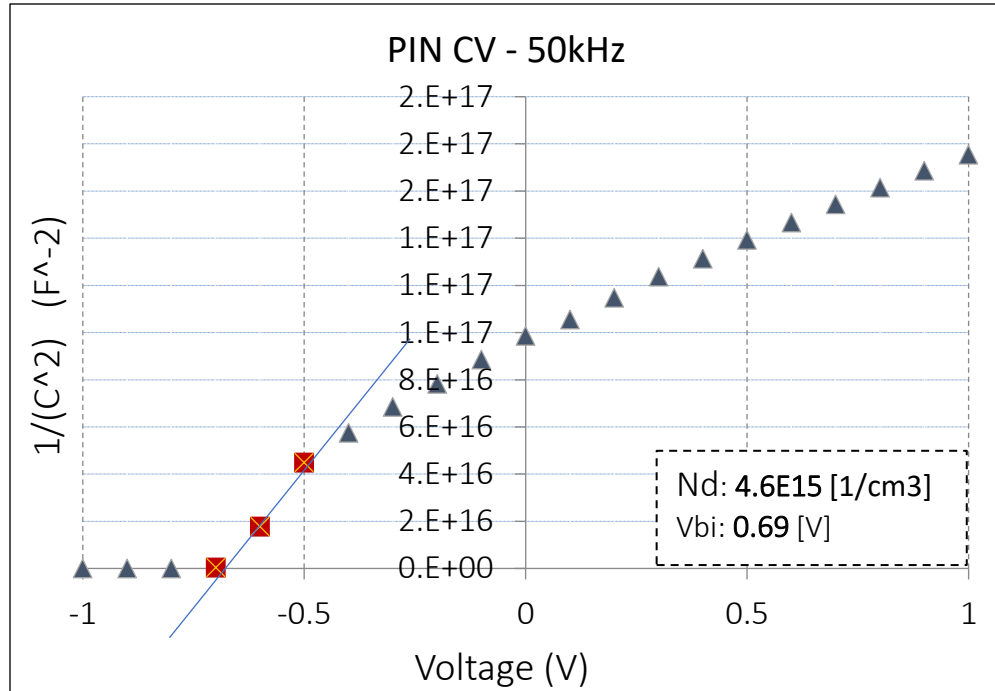


Figure 3.1 PIN device CV results

The PEDOT p-layer used in our PIN devices is known to yield fairly low shunt resistances ($\sim 4\text{k}\Omega$). The reader will be keen to note the secondary slope present at reverse biases. This is due to the trap DOS latent in the sample coupling into the measurement. Thus the “doping” yielded by this secondary slope returns the superposition of donor doping plus the trap DOS ($N_D + N_T$), and therefore is erroneous. For this reason, the left-most linear fit in the linear fit is taken to represent exclusively donor doping, and not the trap DOS.

NIP CV Measurement

Again, the NIP device rested in absence of light for 30 minutes prior to measurement, allowing any latent photogenerated carriers to recombine. The device was then swept from -1V (forward bias) to +1V (reverse bias), with 100mV steps in-between each sample. A small-signal frequency of 200kHz was employed. The measurement results are presented below in figure 3.2:

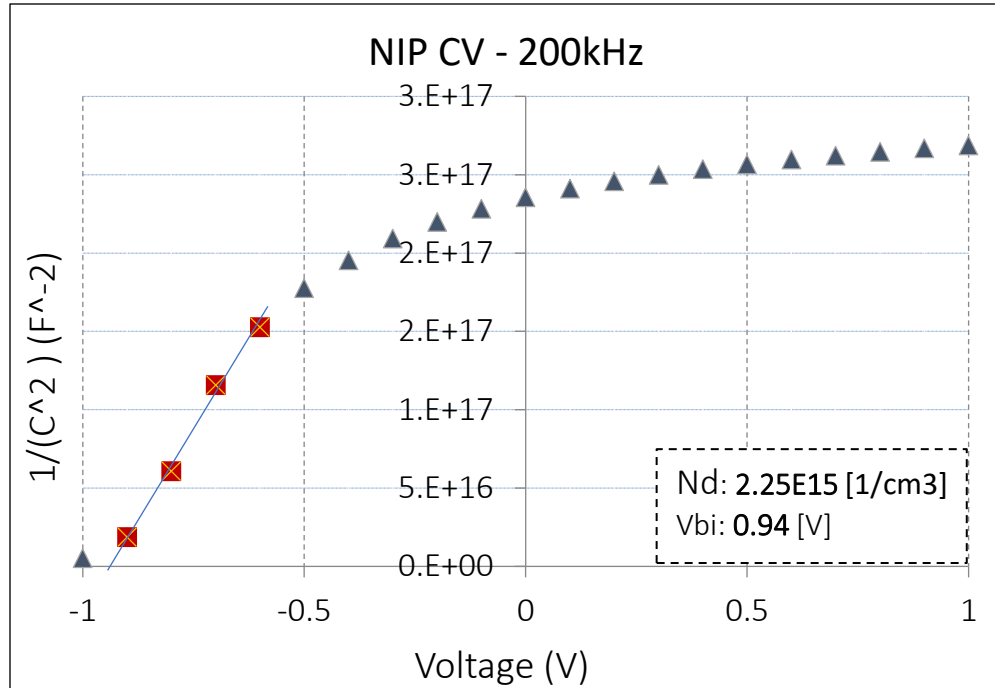


Figure 3.2 NIP device CV results

The reader will note that in the NIP device above, we find only one linear fit. This is indicative of the quality of the NIP device, particularly the absence of trap states. In the results section below, this reduced density of trap states will be reflected in the obtained $\mu\text{-}\tau$ product. From the data sets above (figures 3.1 and 3.2), we obtain the doping concentrations and built-in voltages for our two devices of interest.

EQE Vs. λ

Ultimately, we must experimentally determine the IQE of our devices at all wavelengths of interest. This can be accomplished by first measuring device external quantum efficiency (EQE), and then adjusting values for reflections to yield IQE. Our test-bench for measuring EQE as we sweep incident light wavelength is given below in figure 3.3:

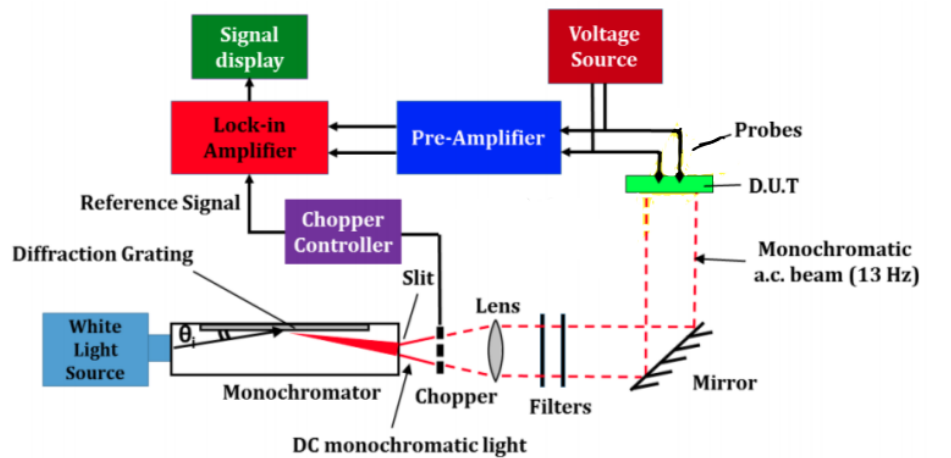


Figure 3.3 EQE test-bench

Firstly, a broadband, Tungsten-halogen bulb is used to generate white light, to be filtered for measurement. The broadband light is channeled through the monochromator, which employs diffraction gratings to allow for high selectivity of the passed wavelength. Generally, the user can select the desired wavelength, with approximately ± 1 nm of error. The monochromatic “DC” light is then passed through a chopper - this acts to modulate our sample signal to ~ 13 Hz, such that we can lift it out of the noise floor.

The rapidly diverging monochromatic beam is then parallelized into a collimated beam via a large convex lens. Next, the collimated light passes through a filter array in order to kill harmonics present in the system that would otherwise skew sample data. The following filters are employed over our wavelength sweep:

- [400,580nm] \rightarrow 580nm Low Pass Filter
- [580, 700nm] \rightarrow no optical filter used post-lens
- [700, 900nm] \rightarrow 700 nm High Pass Filter
- [900 - 1100nm] \rightarrow 700 nm High Pass + 900 nm High Pass

The beam is then directed incident the device-under-test (DUT) or onto a reference via a 45° mirror. When measuring device absolute quantum efficiency, it is required to adjust measured DUT values with a reference of known absolute quantum efficiency, as shown below in equation 3.2:

$$EQE_{DUT}(\lambda) = \frac{V_{DUT}(\lambda)}{V_{reference}(\lambda)} \cdot \frac{Area_{Reference}}{Area_{DUT}} \cdot EQE_{Reference}(\lambda) \quad (3.2)$$

The reader will note that the reference and DUT are measured on identical optical paths – as it is critical that the photon flux incident the DUT be identical to that incident the reference, i.e. $\Gamma_{DUT}(\lambda) = \Gamma_{Reference}(\lambda)$. Additionally, a 2mm aperture is employed to ensure the illuminated area is identical between the reference and the DUT.

Finally, the signal from the reference / DUT is collected into a zero-impedance current preamplifier, where it is buffered and amplified, and mixed into the lock-in amplifier. Traditionally, lock-in amplifiers are employed when the desired signal is buried in background noise. As described above, our incident beam is modulated at ~13Hz by the chopper. This ~13Hz signal is fed into the lock-in amplifier as the reference signal (not to be confused with the reference photocell signal). The lock-in amplifier is then able to “lock in” to the ~13Hz component of the sample/reference cell signal, and provide users with a stable DUT signal.

PIN EQE Measurement

In the process described above, we obtain the external quantum efficiency for the PIN device used in this study. The results are shown below in figure 3.4:

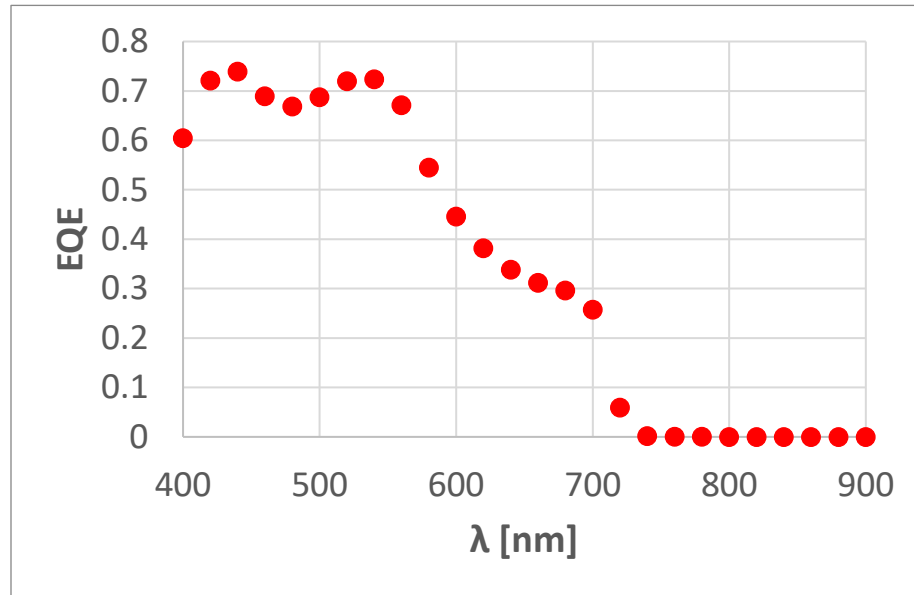


Figure 3.4 EQE Vs. Wavelength, PIN device

NIP EQE Measurement

Similarly, we obtain the external quantum efficiency for the NIP device used in this study. The results are shown below in figure 3.5:

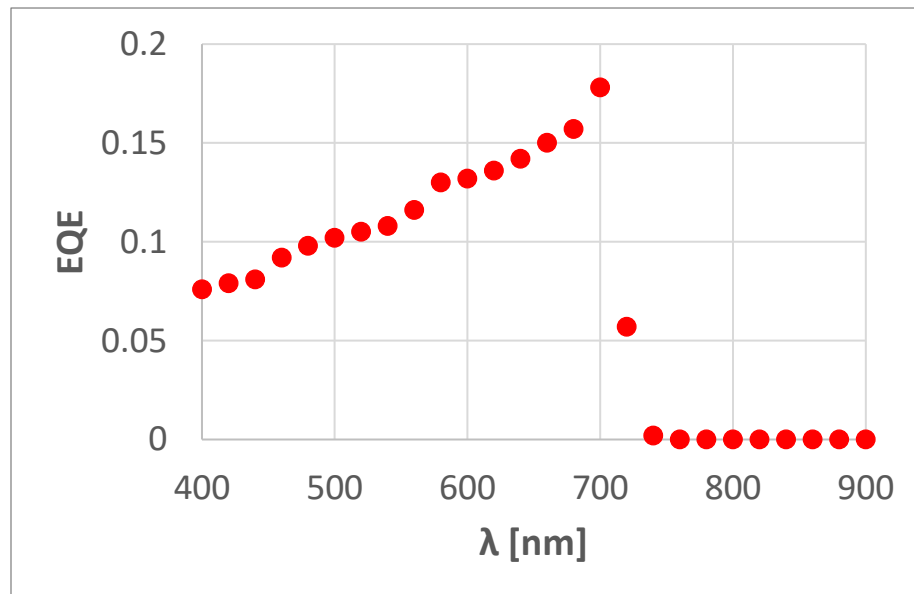


Figure 3.5 EQE Vs. Wavelength, NIP device

The reader will note the profound difference, both in shape and magnitude, between the EQE of the two devices. Shape is intuitively explained by the nature of

Cadmium Selenide's absorption spectrum. At shorter wavelengths, the absorption coefficient α is high – therefore high energy photons are absorbed close to their plane of incidence.

In the PIN device, this means that at short wavelengths, photogenerated minority holes only have to travel a short distance until they are collected at the p-layer – therefore the EQE is high at short wavelengths for PIN devices. As the wavelength increases, the absorption occurs deeper and deeper in the CdSe layer, and therefore minority holes must travel greater distances for collection. The 'deep' holes have a higher probability of recombining before being collected. Figure 3.4 confirms this, as longer wavelengths yield lower EQEs for the PIN structure.

Just the opposite is true in the NIP device. Short wavelengths are absorbed near the n-layer, and therefore minority holes must traverse the entire CdSe layer to be collected at the p-layer. These holes have a high probability of recombining prior to collection, and therefore the associated EQE at short wavelengths is low for the NIP structure. The longer wavelengths penetrate deeper, and therefore are absorbed nearer to the p-layer – thus holes generated here have a higher probability of collection and EQE. This phenomena is demonstrated above in figure 3.5.

Clearly, the PIN device is much more efficient than the NIP device, in terms of overall EQE. While overall device efficiency, and its subsequent improvement, are a focus of our group, the purpose of this thesis is to observe the fundamental transport and characteristic $\mu\text{-}\tau$ product of CdSe absorbing layers. Therefore, the efforts and progress made in device engineering (improving HTLs and ETLs, fabrication

improvements, etc.) will not be discussed here. These interesting topics deserve (and will receive) their own theses and analysis.

Reflectivity

Lastly, sample reflectivity is required to extract the IQE data from the EQE data set presented above. The relationship between IQE and EQE is defined below in equation 3.3:

$$IQE(\lambda) = \frac{EQE(\lambda)}{1-R(\lambda)} \quad (3.3)$$

Note that equation 3.3 above presumes zero transmission thru the device. In other words, we approximate that any light not reflected by the sample, must be absorbed within the sample. This is not an unreasonable postulation, given the characteristically high extinction coefficient of CdSe, combined with the fact that both samples are relatively thick.

A *Filmetrics F20 thin film analyzer* is employed to measure the reflectivity of our devices. Generally, the F20 system is equipped to not only obtain reflectivity data, but also calculate film thicknesses, refractive indices, or extinction coefficients – depending on the user’s previous knowledge of their sample. However, for our simple requirements, we only need raw reflection. Figure 3.6 below illustrates the general physics of the measurement:

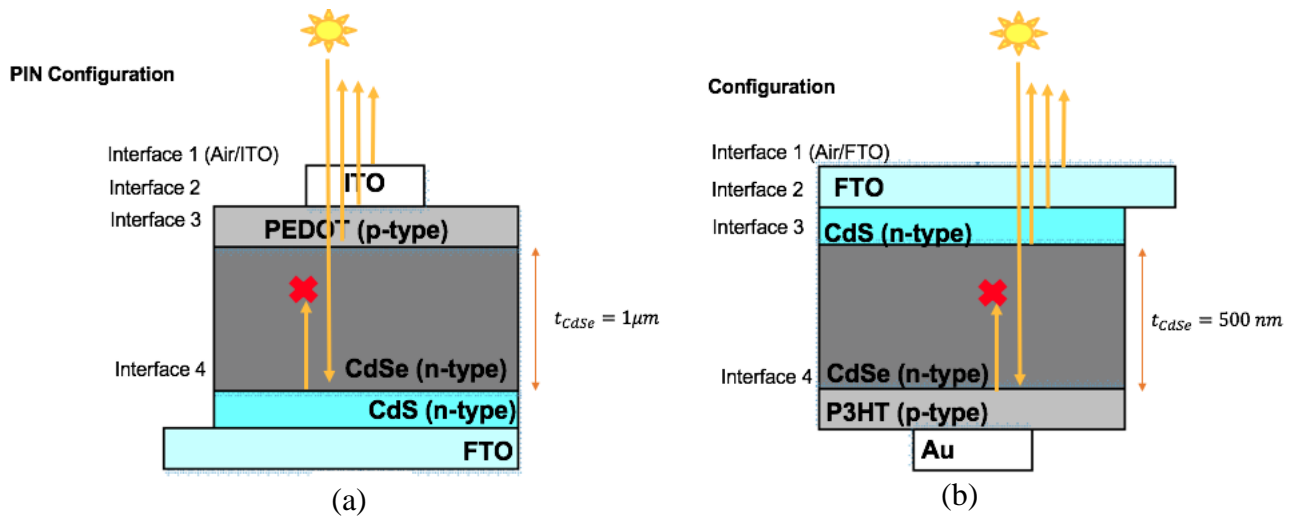


Figure 3.6 Dominating reflections in Filmetrics measurement (a) PIN, (b) NIP

The reader will note that the Filmetrics system only radiates and collects light that is perpendicular to the sample plane. For our purposes, this simply means we can disregard the possibility of total internal reflection (TIR).

It is also worth noting that we expect very little reflection from interface 4, detailed in the figure above. Again, this is because of CdSe's high extinction coefficient. Any light reflected at interface 4 must travel back thru the full thickness of the absorption layer, effectively doubling the thickness of the CdSe layer. This is readily apparent when one inspects equation 2.9.

PIN Reflectivity

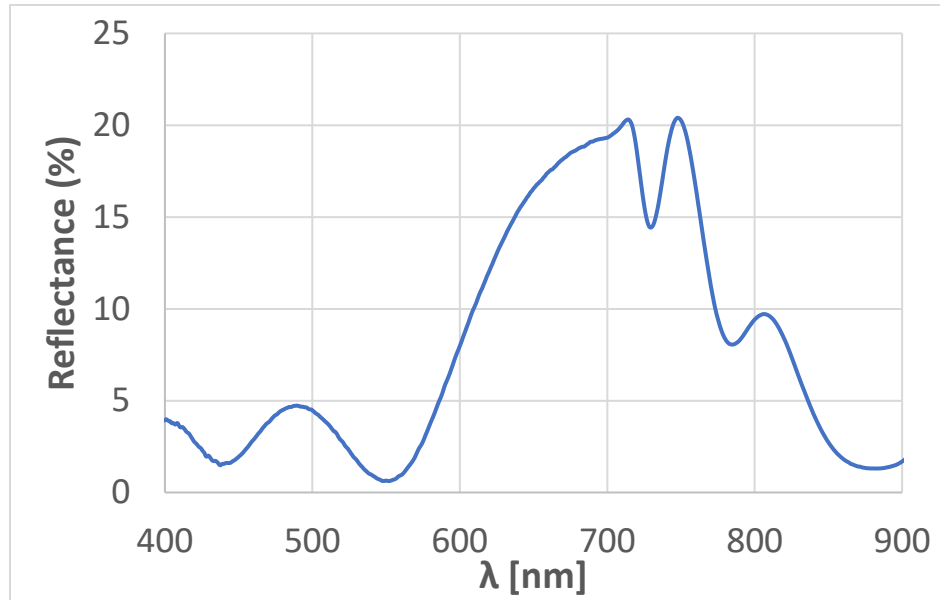


Figure 3.7 PIN device reflectivity

Note – recall the EQE shape of the PIN device in figure 3.4. Peaks and troughs (in the 400nm to 600nm range) in EQE correspond to troughs and peaks in the sample reflectivity.

NIP Reflectivity

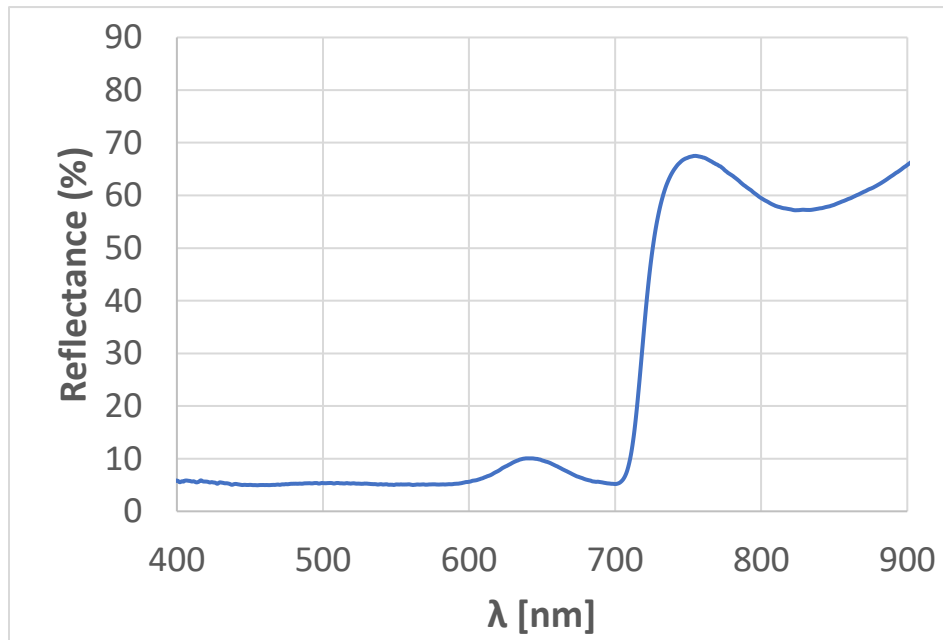


Figure 3.8 NIP device reflectivity

At long wavelengths, both devices demonstrate complex interference patterns, typical of multi-film devices. However, as stated before, at our wavelengths of interest greatly simplify the situation. At 500, 600, and 700nm, we neglect any transmission through the device due to CdSe's extinction coefficient at these wavelengths. Therefore, equation 3.3 holds for our applications and we can evaluate for the IQEs of our devices. Finally, via combining our EQE observations with the reflectivity data presented above, it is now possible to determine device IQE at all wavelengths of interest.

IQE Vs. V_{bias}

In order to determine the accuracy of our model, and obtain a mu-tau of best fit, we require an experimental data set to compare the model values to. Our model expresses IQE as a function of the applied bias, therefore must be compared against $IQE_{experimental}$ vs. $V_{bias,experimental}$. As mentioned above, IQE can be rather difficult to measure experimentally, but EQE is much simpler. One simple observation allows us to do so:

$$\frac{IQE_V(\lambda)}{IQE_{0V}(\lambda)} = \frac{EQE_V(\lambda)}{EQE_{0V}(\lambda)} \quad (3.4)$$

By measuring EQE at a set of voltages, and then dividing the entire data set by the unbiased case, we effectively divide out the contribution of reflection, at a given wavelength. With the reflection term eliminated, the ratio is clearly equivalent to its IQE counterpart. This EQE measurement is performed using the same test-bench and equipment described in figure 3.3 above.

For each of our devices, we sweep thru a set of bias voltages – from +0.5V reverse bias, to -0.5 forward bias, with steps of 0.1V. We repeat this sweep at our 3 wavelengths of interest: 500, 600, and 700nm. Then, just as indicated by equation 3.4

above, we divide each sample by the unbiased value. The results are shown below, in figures 3.9 and 3.10:

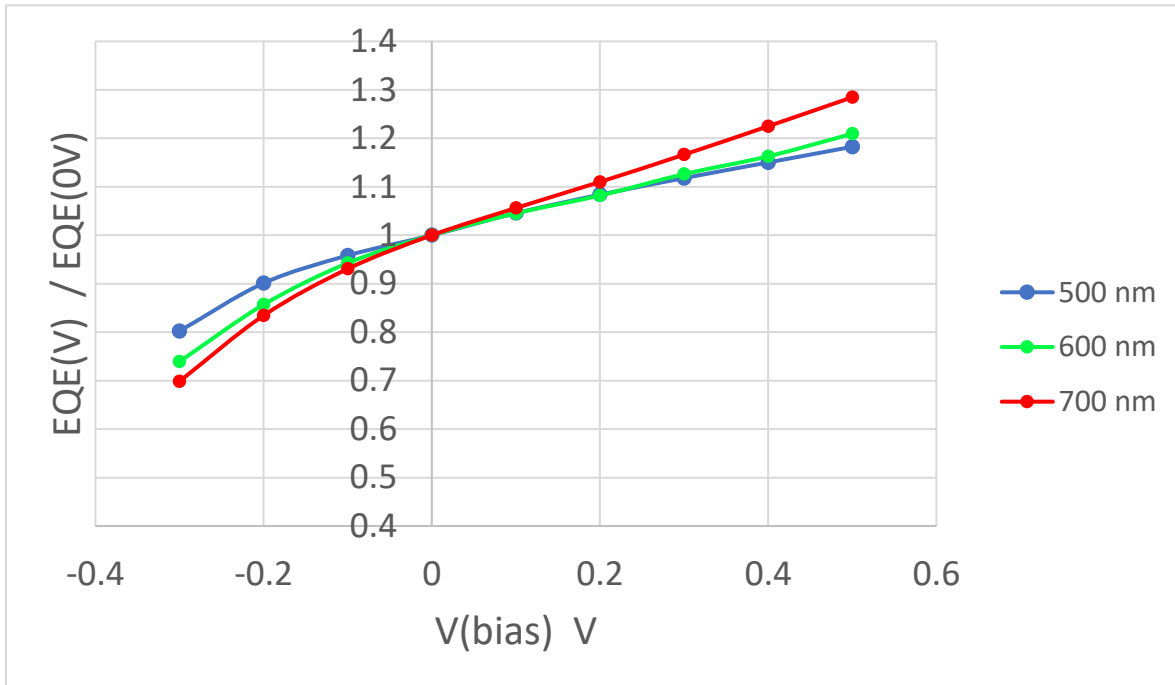


Figure 3.9 EQE ratio Vs. voltage, PIN device

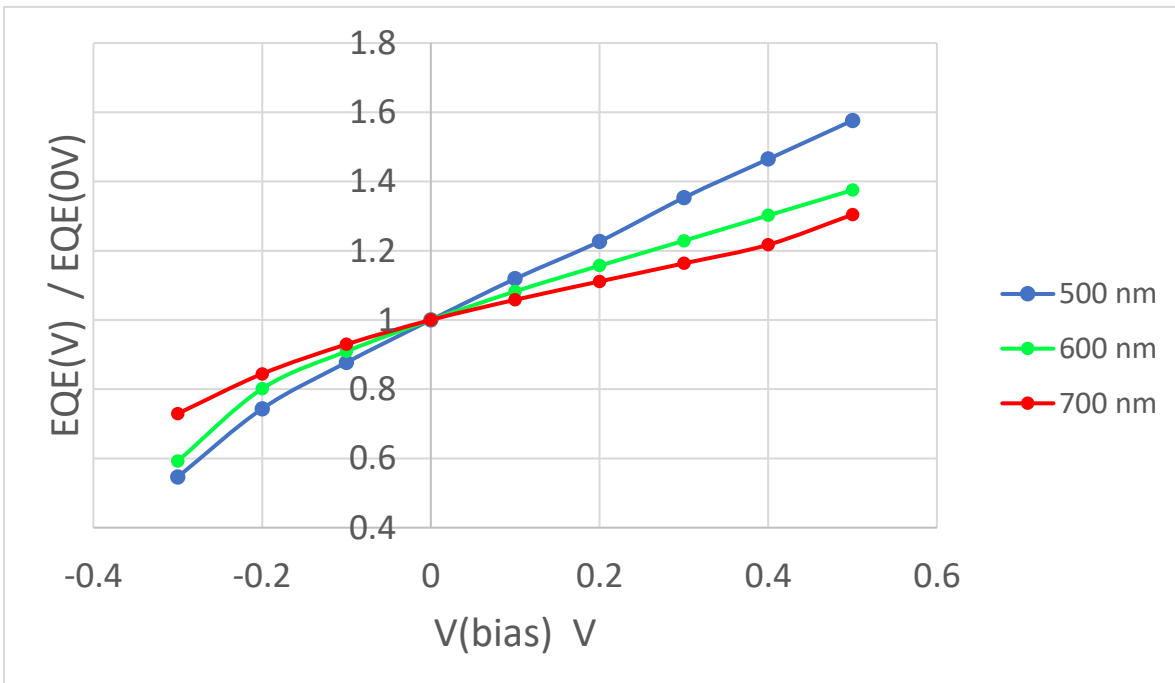


Figure 3.10 EQE ratio Vs. voltage, NIP device

Further applying equation 3.4 above, we need only multiply our ratio values by the known IQE to obtain experimental IQE vs. $V(\text{bias})$ curves, as shown below in figures 3.11 and 3.12:

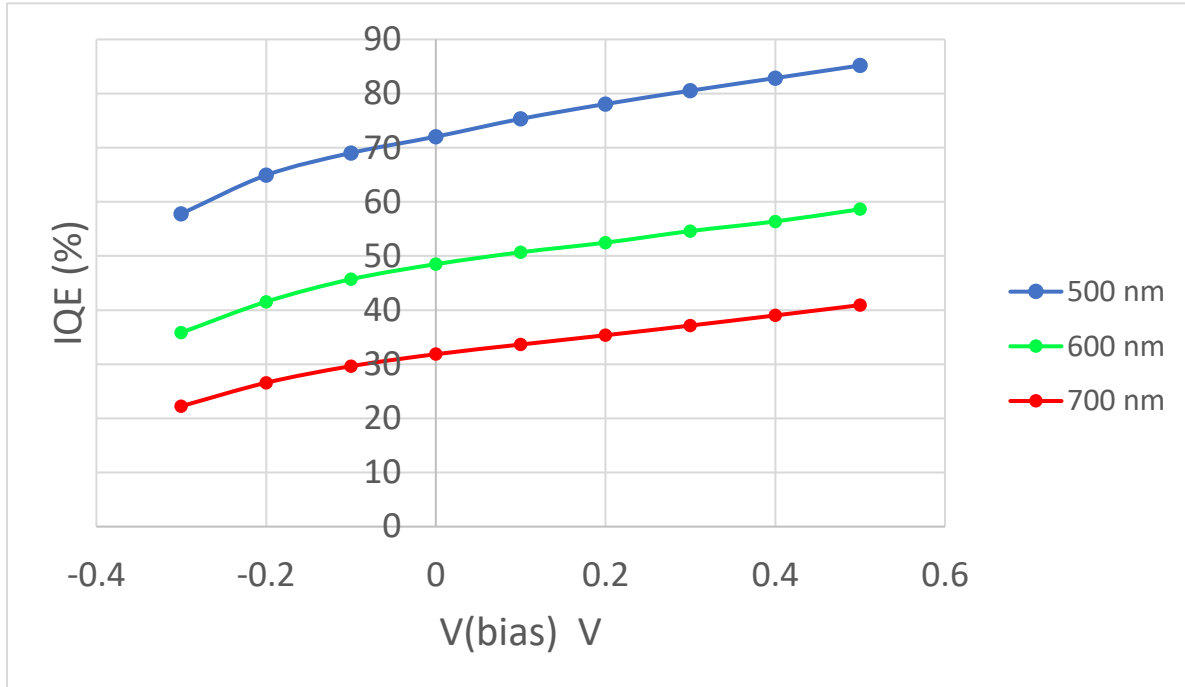


Figure 3.11 IQE Vs. voltage, PIN device

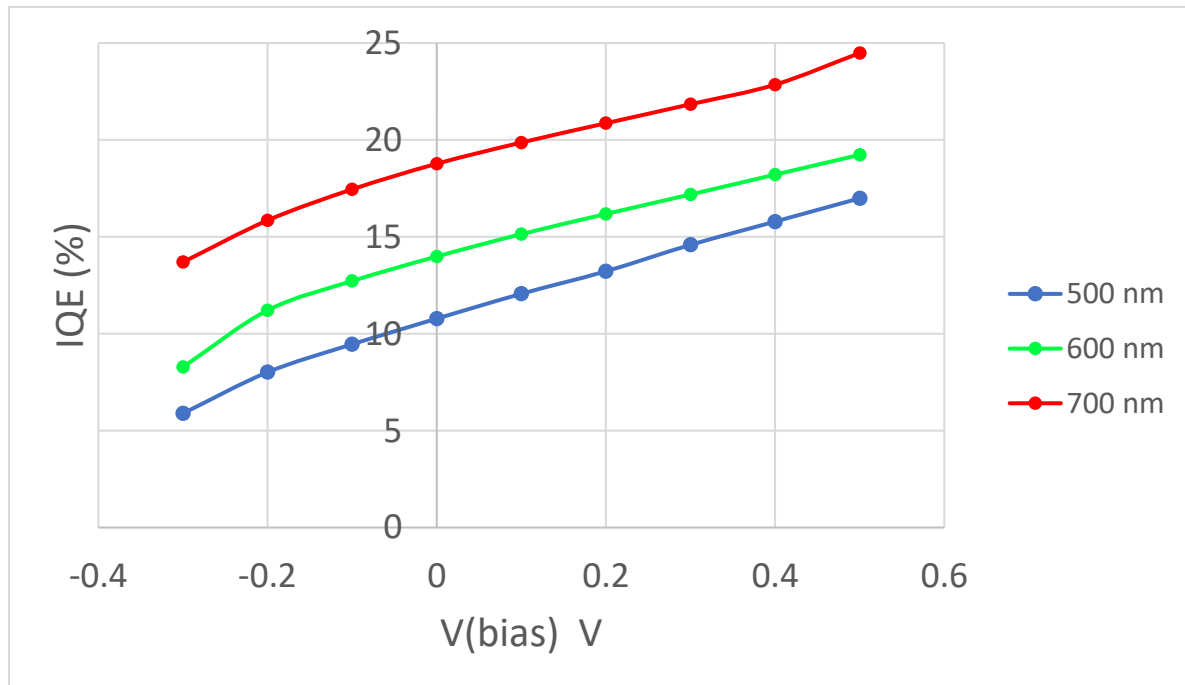


Figure 3.12 IQE Vs. voltage, NIP device

Finally, with figures 3.11 and 3.12, we arrive at an experimental data set with which we can compare our model expression.

CHAPTER 4. RESULTS

Fitting - Initial Impressions

Taking the aggregate data collected in the measurement stage above – built-in voltages, CdSe donor doping concentrations, sample thicknesses, sample reflectivity's, and literature-derived absorption coefficients – all of these necessary device parameters are taken as inputs into our MATLAB model. The model, executing the expressions given in the theory chapter above, rasters thru a range of mu-tau values (all mu-tau values are in the units of $\frac{\mu m^2}{V}$), and overlays the plots of $[IQE_{experimental} vs. V_{bias}]$ with $[IQE_{model} vs. V_{simulated bias}]$ as shown below:

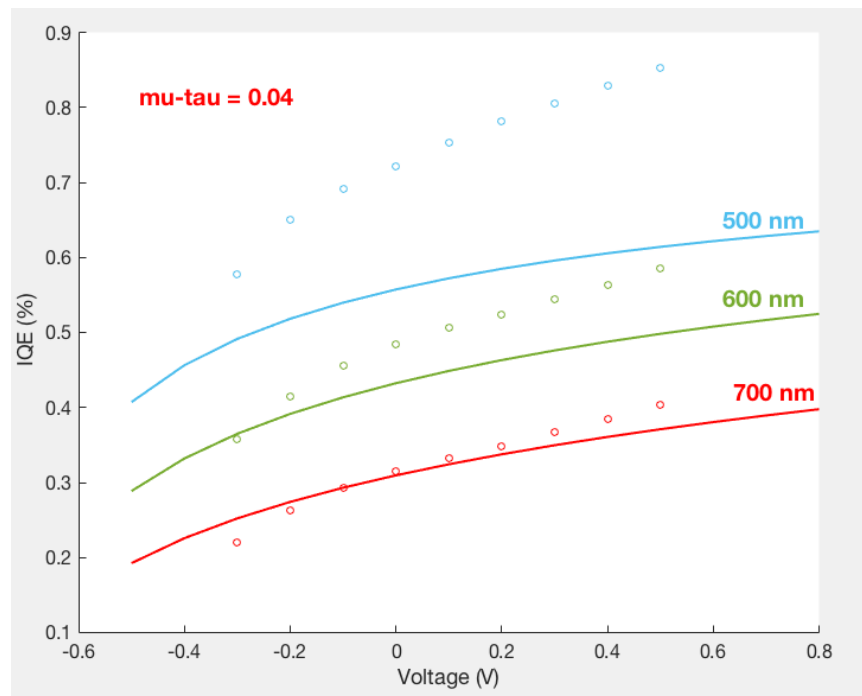


Figure 4.1 model fits at mu-tau = 0.04, PIN device

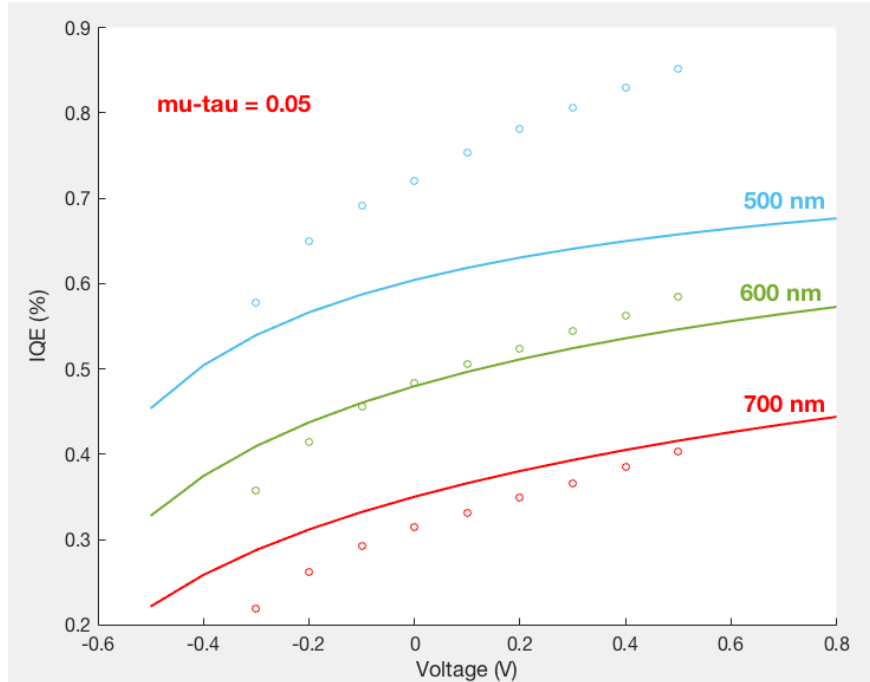


Figure 4.2 model fits at $\mu\text{-tau} = 0.05$, PIN device

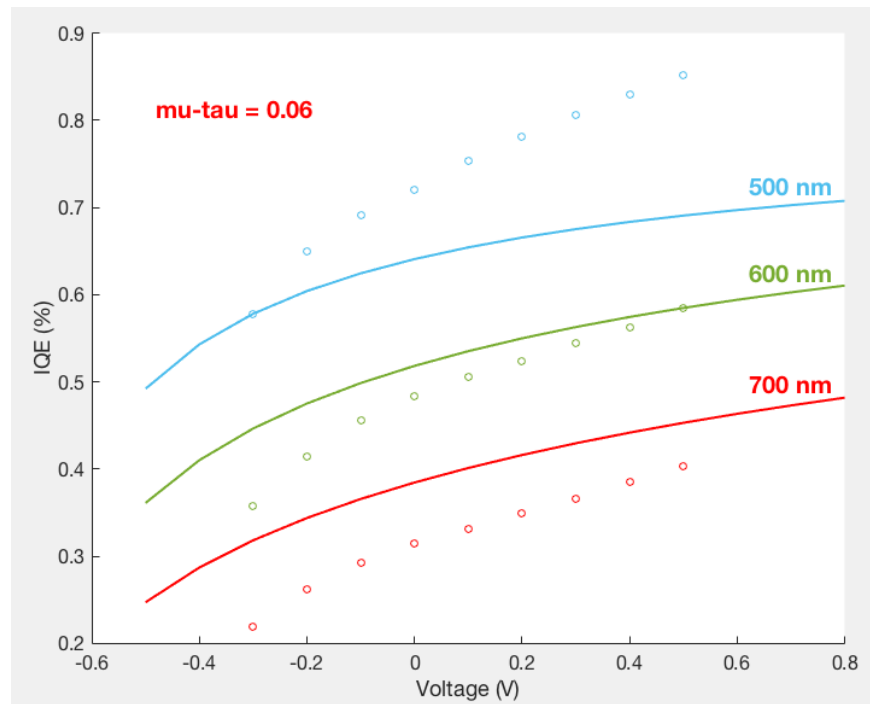


Figure 4.3 model fits at $\mu\text{-tau} = 0.06$, PIN device

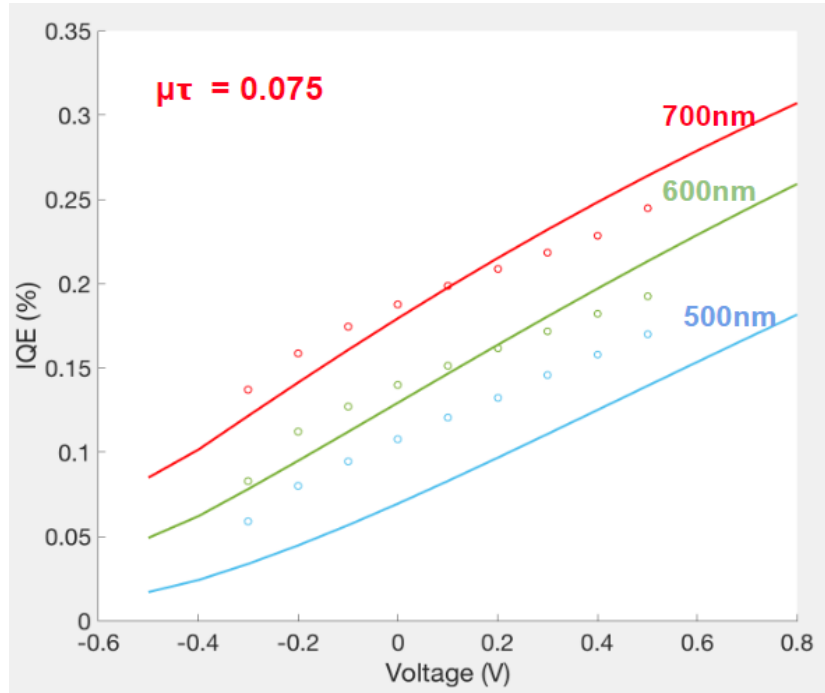


Figure 4.4 model fits at $\mu\tau = 0.075$, NIP device

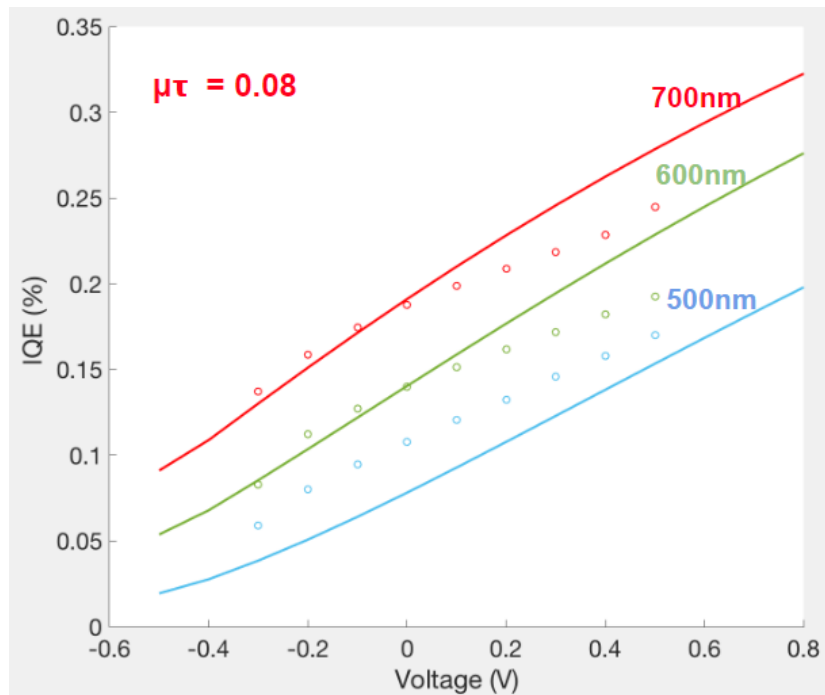


Figure 4.5 model fits at $\mu\tau = 0.08$, NIP device

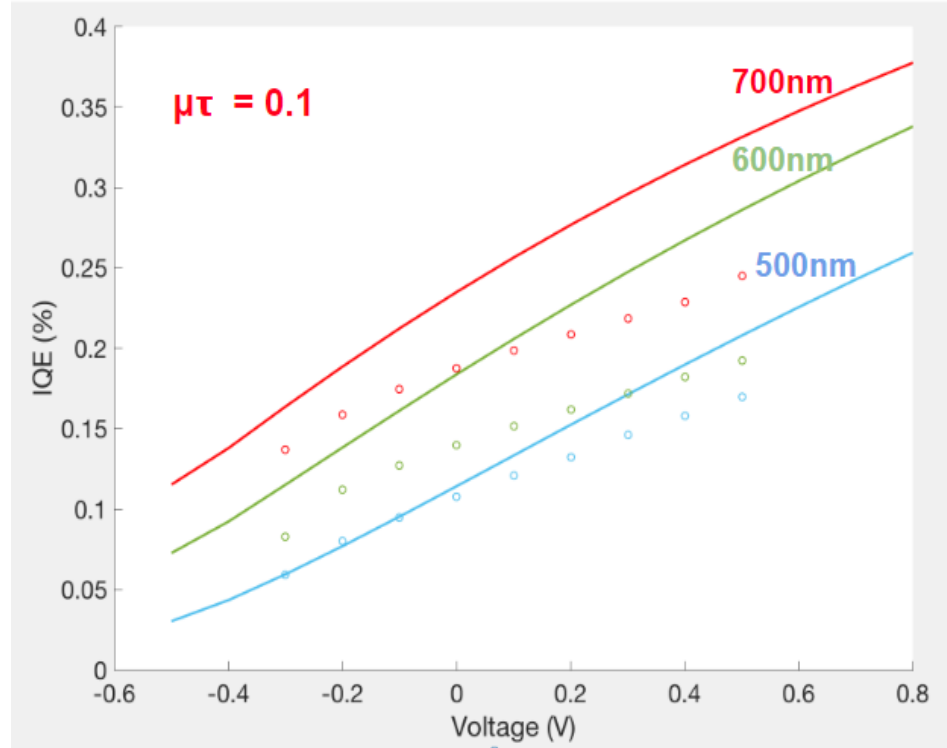


Figure 4.6 model fits at $\mu\tau = 0.10$, NIP device

Discussion

By sweeping the $\mu\tau$ parameter over a range of values and inspecting the fit at each $\mu\tau$, we visually obtain a $\mu\tau$ of best fit for each of the two devices explored above. We find that the PIN device is best characterized by a $\mu_p\tau_p \approx 0.05 \frac{\mu\text{m}^2}{\text{V}}$, while the NIP device is best characterized by a $\mu_p\tau_p \approx 0.075 \frac{\mu\text{m}^2}{\text{V}}$.

We also note that for both devices, the fit at $\lambda = 500 \text{ nm}$ is poor. We believe this to be due to the absorption coefficient $[\alpha_{\text{CdSe}}(\lambda = 500\text{nm})]$ value employed at this wavelength. Our model is *heavily* dependent on the value of absorption coefficient used in calculation. As stated in previous sections, absorption coefficient values for CdSe are taken from existing literature [3, 4]. In studies of both single crystal CdSe, and thin film CdSe, authors largely agree upon the absorption coefficient values at 600nm and 700nm. However, we find that the absorption coefficient at 500 nm is sparsely defined in

literature [3, 4, 5]. Any potential error in the literature-derived value of $\alpha_{CdSe,500nm}$ would have significant impacts on the fits provided above.

Generally, we note that the model shape matches the experimental data for both PIN and NIP devices. We assess the accuracy of the analysis by computing the standard deviation (σ) between the corresponding sets of data (i.e. deviation between experiment and simulated curves, at a given wavelength). At the mu-tau of best fit for the above PIN device, we find (in terms of IQE) $\sigma_{700nm, PIN} = 3.86 \%$ and $\sigma_{600nm, PIN} = 2.61 \%$, while for the NIP devices, deviations are evaluated as $\sigma_{700nm, NIP} = 1.40 \%$ and $\sigma_{600nm, NIP} = 1.25 \%$.

Above, we demonstrate our ability to deduce a mu-tau of best fit for devices of both PIN and NIP architectures. However, given the vast number of structural and process differences between the two devices presented above, there is no reason to think that the mu-tau values should be equivalent between the NIP and PIN devices. In fact, according to the CV measurements between the two devices, it follows that the NIP is characterized by a higher mu-tau than the PIN device. This is suggested by the increased density of traps present in the PIN device (given by the lack of saturation at higher reverse biases in its CV curve).

Thus far, we have merely demonstrated our ability to determine a given mu-tau for a given device. While this is powerful in terms of device characterization, the true power of our model is rooted in its ability to tell us how certain processes and fabrication techniques impact the quality of our CdSe absorption layer, and therefore the effectiveness of our devices as solar cells. In the section to follow, we demonstrate how

our mu-tau determination be used as a probe to reveal the effect of CdSe fabrication/processing techniques.

CdSe Fabrication Effects on $\mu\tau$

For 3 PIN devices (similar to the PIN device outlined in this thesis), we test the impact of post-deposition annealing on device $\mu_p\tau_p$. These 3 devices are fabricated in *identical* conditions, other than the conditions in which the device is annealed, after the CdSe absorption layer is thermally evaporated onto the film. The 3 post-annealing processes are as follows:

- Device 1 – Post-annealed at 450°C for 2 hours
- Device 2 – Post-annealed at 450°C for 10 hours
- Device 3 - $CdCl_2$ spun on, then post-annealed at 450°C for 10 hours

Without belaboring this discussion, we have independently studied the effects of these three processes in terms of sub-bandgap absorption. Our results have shown a significant reduction of sub-gap trap states due to post-annealing at 450°C. In general, our sub-gap absorption measurements have confirmed the following:

- 1.) Post-annealing at 450°C significantly reduces the sub-gap density-of-states (DOS), and increases device performance
- 2.) No notable difference in sub-gap DOS between treatments at 450°C for 2 hours, and treatments at 450°C for 10 hours
- 3.) $CdCl_2$ spun on to devices just prior to post-annealing significantly reduces the sub-band DOS

Based on the independent observations of trap DOS above, we theorize that the $\mu\tau$ values characterizing devices 1 and 2 should be similar, while the $\mu\tau$ of device 3 should be improved above the others, i.e. we postulate the following:

$$\mu_p \tau_p, \text{ Device 1} \approx \mu_p \tau_p, \text{ Device 2} < \mu_p \tau_p, \text{ Device 3}$$

All three devices are characterized in the methods described above, with CV, EQE, and reflectivity measurements. The values obtained in these measurements are taken as inputs into our model, and $\mu_p \tau_p$ is swept thru a range of values, as shown below:

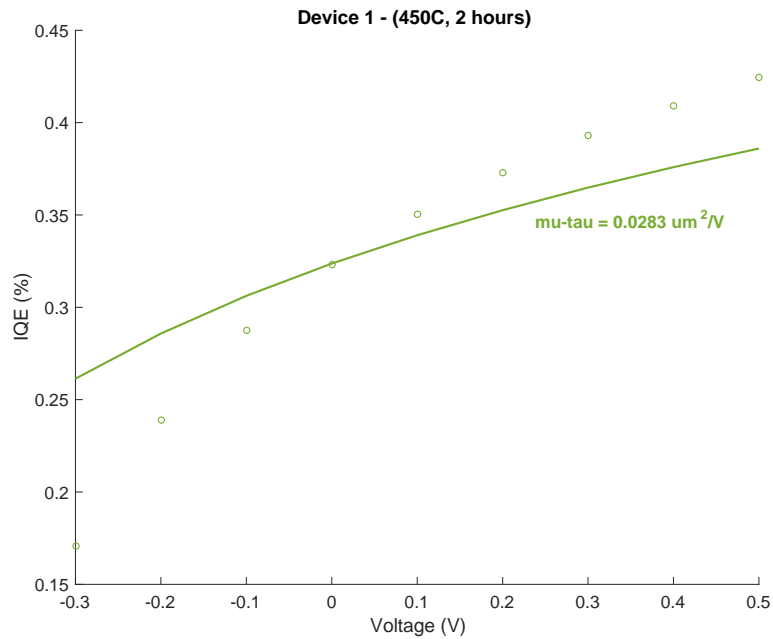


Figure 4.7 $\mu\tau$ yielding best fit for device 1

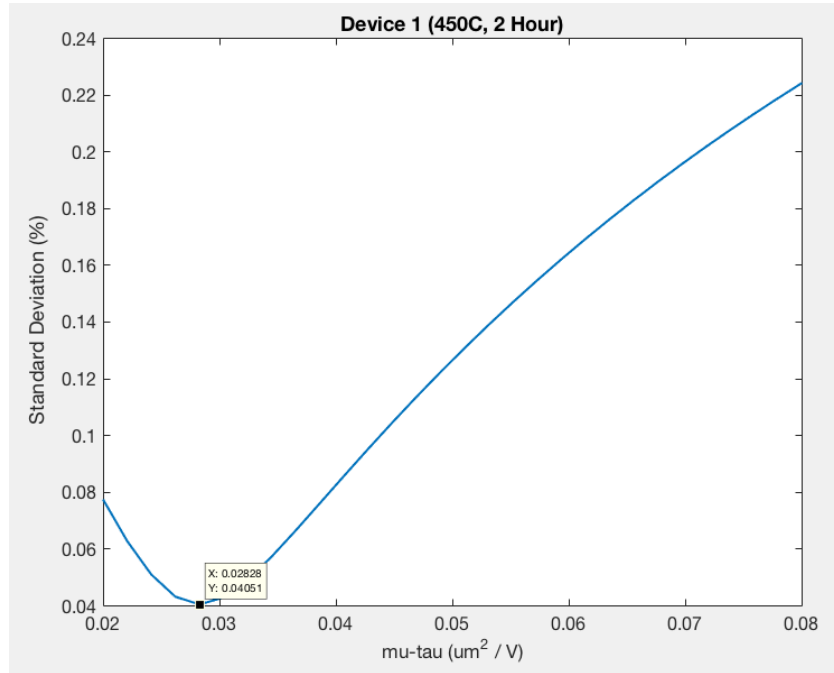


Figure 4.8 standard deviation for device 1 fitting

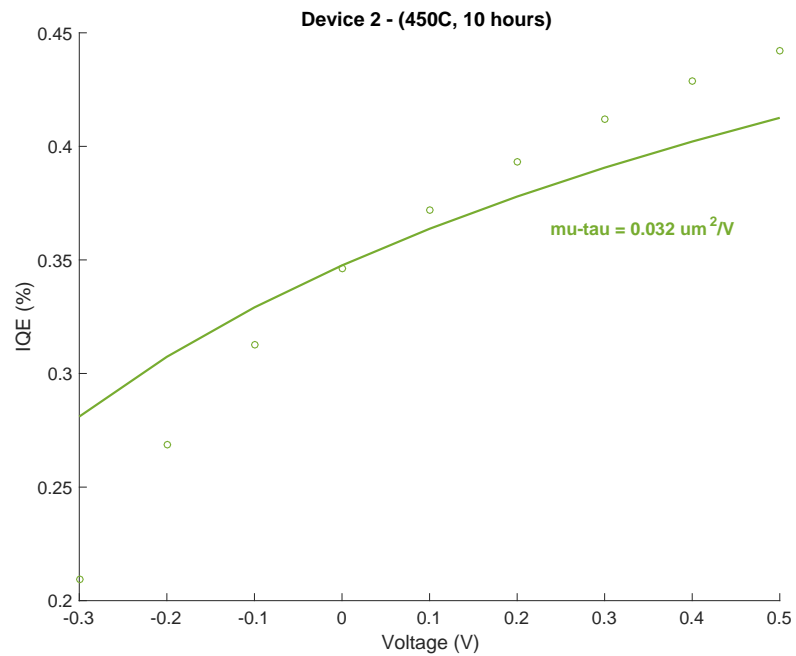


Figure 4.9 mu-tau yielding best fit for device 2

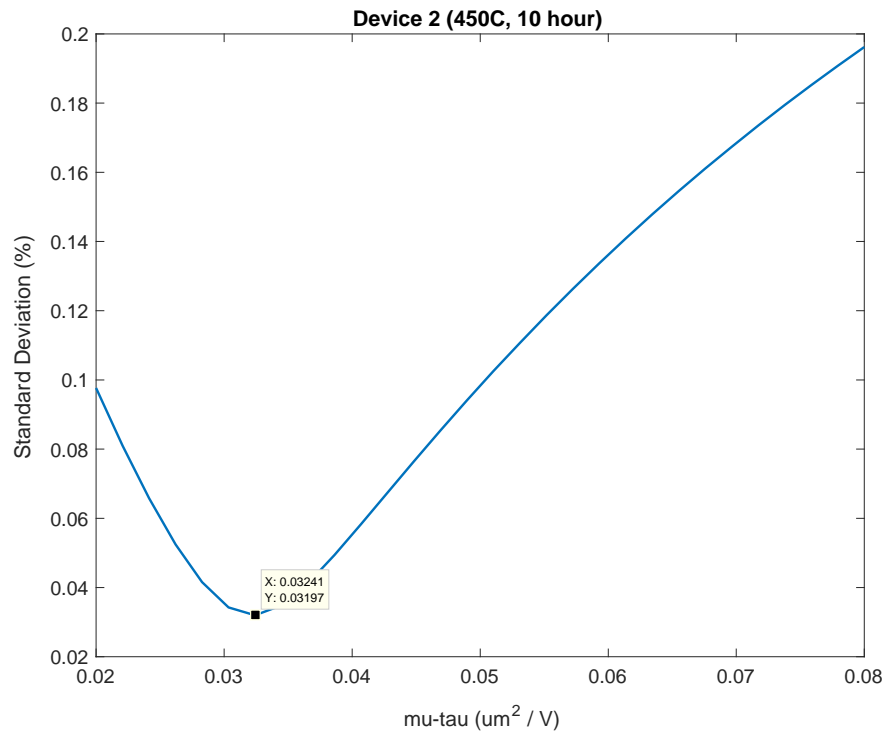


Figure 4.10 standard deviation for device 2 fitting

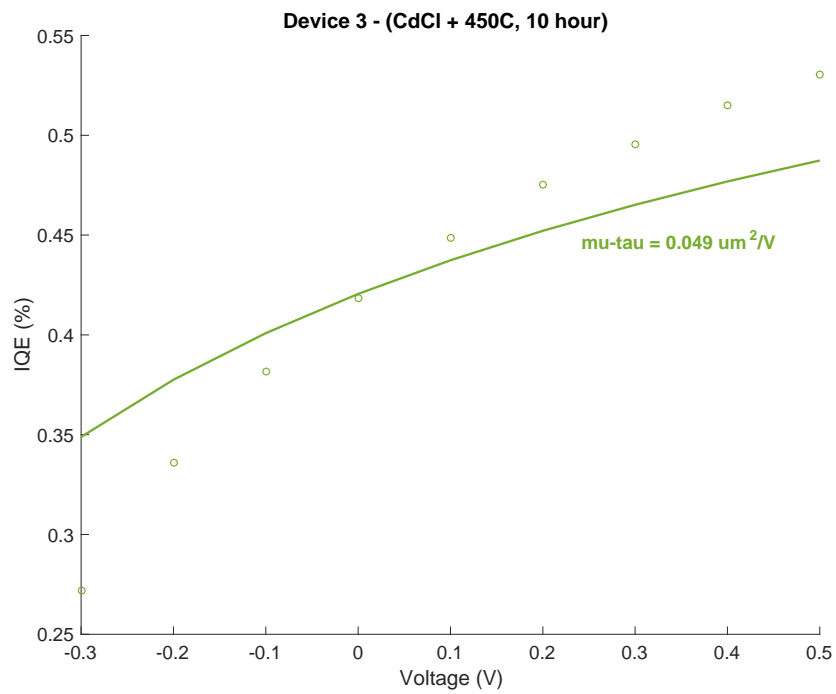


Figure 4.11 mu-tau yielding best fit for device 3

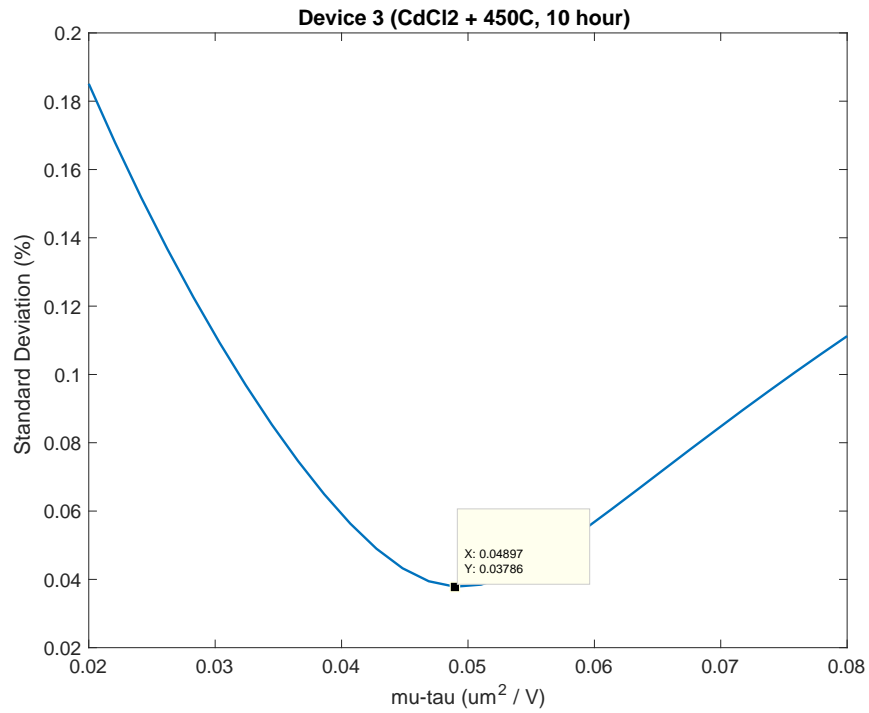


Figure 4.12 standard deviation for device 3 fitting

Just as we suspected, we find the $\mu_p\tau_p$ relationship between devices 1, 2, and 3 to shown the same trend as our sub-gap absorption data. We find that devices characterized by low trap DOS achieve significantly higher mu-tau products than devices whose sub-gap DOS is high. Additionally, in devices where the sub-gap DOS stays the same (device 1 and 2), the mu-tau product characterizing those devices are comparable.

CHAPTER 5. CONCLUSION

This thesis presented a novel and simple method by which minority carrier transport within CdSe solar cells can be modeled. The model expression derived proves to be useful across multiple device architectures (PIN, NIP). Further, it is revealed that by adjusting the $\mu\tau$ product employed in simulated curves, the user is empowered to obtain a $\mu\tau$ product of best fit for the device – a parameter of great interest in characterizing thin film solar cell performance.

For all samples tested, we find the model output to be highly sensitive to the literature-derived absorption coefficient utilized, and the characteristic sub-gap density of trap states of the particular sample. Additionally, samples characterized by low shunt resistances prove to induce nontrivial error into both the CV and IQE v. V measurements. While fit error easily grows with any uncertainty in absorption coefficient employed, we find standard deviation to be less than 5% (in terms of IQE) for all curves obtained. Additionally, we find our CdSe devices to be characterized by minority-carrier $\mu\tau$ values on the order of $\approx 5 \cdot 10^{-10} [\frac{cm^2}{v}]$, at times approaching values of $\approx 1 \cdot 10^{-9} [\frac{cm^2}{v}]$ – depending upon device structure and overall quality of device (sub-gap DOS, etc.).

While certainly fits can be improved by adding additional terms and complexity to the model expression, we find that reasonably useful conclusions regarding the carrier transport of CdSe devices can be made with our model as it stands. Additionally, the simplistic nature of this model allows for ease of deployment - experimentally, the model requires only easily obtainable device parameters to generate fits. This simplicity and ease of deployment enables users to quickly characterize the transport of CdSe devices in a novel and insightful manner.

CHAPTER 6. REFERENCES

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